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A SAMPLING CONTROLLER FOR A MULTIPLEXED ANALOG-TO-DIGITAL CONVERTER

BY

GERALD ALVIN KIFFIAK

A THESIS

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FACULTY OF GRADUATE STUDIES

The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research, for acceptance, a thesis entitled "A Sampling Controller for a Multiplexed Analog-to-Digital Converter" submitted by Gerald Alvin Kiffiak in partial fulfilment of the requirements for the degree of Master of Science.

ABSTRACT

This thesis describes a device which permits independent sampling rates for each channel of a 16 channel multiplexed analog-to-digital converter. Therefore, the Sampling Controller, as it is called, makes the 16 channel converter appear like 16 single channel analog-to-digital converters. This versatility is helpful in real-time analysis where it is important to minimize the quantity of superfluous data acquired by the computer. Each channel may be sampled at the appropriate regular or irregular rate for the associated signal.

The Sampling Controller is particularly useful in the acquisition of neuroelectric and myoelectric data. This data, which is in the form of a train of action potentials, can be reduced to peak values and interpeak time intervals.

The Sampling Controller was successfully tested using an analog-to-digital converter and a small computer.

ACKNOWLEDGEMENTS

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Chapter 1

INTRODUCTION

1-1 The Problem

The digital computer's ability to quickly perform complex operations on huge quantities of data has made it valuable in many situations. Research in the sciences is certainly one of the areas where the computer has become increasingly important. This is especially true in the life sciences where statistical analysis is frequently required.

Recently, as minicomputers have become more common in the laboratory, the appreciation for real-time analysis has grown.[1] The advantages of seeing the results of analysis displayed, during an experiment, are numerous. For example, any general trend in a calculated parameter is immediately obvious. Also, the effect of an applied disturbance to the experiment can be quickly assessed. If biological preparations are involved, it is imperative that the experiment be completed as quickly as possible since live tissue tends to degenerate with time. In such cases, real-time computing can be invaluable in speeding up the experimental procedure.

Unfortunately, there are situations where it is not possible to use a computer in real-time. This may happen if the rate at which the computations can be performed on the input data is less than the rate at which that data is acquired. In other words, the quantity of input data may be too large, or the level of computational complexity

may be too high. In either case, the computer falls behind in the task and is finally overwhelmed.

The purpose of this work was to design a flexible data acquisition system that facilitates real-time analysis. In many instances this system can be used to reduce the quantity of data which reaches the computer. In other cases, operations can be done on some types of data before analog-to-digital conversion to spare the computer much calculation. The reduction of a train of action potentials to peak values and interpeak intervals is an example. The data acquisition system is composed of an ordinary multiplexed analog-to-digital converter, and a Sampling Controller. The Sampling Controller is the subject of this thesis.

1-2 A Data Acquisition System

A data acquisition system, that is in common use as a peripheral for a digital computer, is depicted in Figure 1-1. Usually, since more than one channel is to be digitized, an analog multiplexer must be used with the analog-to-digital converter. One analog-to-digital converter per channel is more flexible than the multiplexer arrangement but cost factors presently make the multiplexer scheme more practical.

There are at least three drawbacks to the multiplexer-converter combination. Each of these stems from the fact that no two channels may be converted simultaneously. First, the maximum sampling rate of a particular channel is reduced by multiplexing. If the multiplexer has N analog channels, and the conversion rate of the analog-to-digital converter is R samples per second, then the maximum sampling rate for one channel is R/N samples per second. Second, it is never possible to

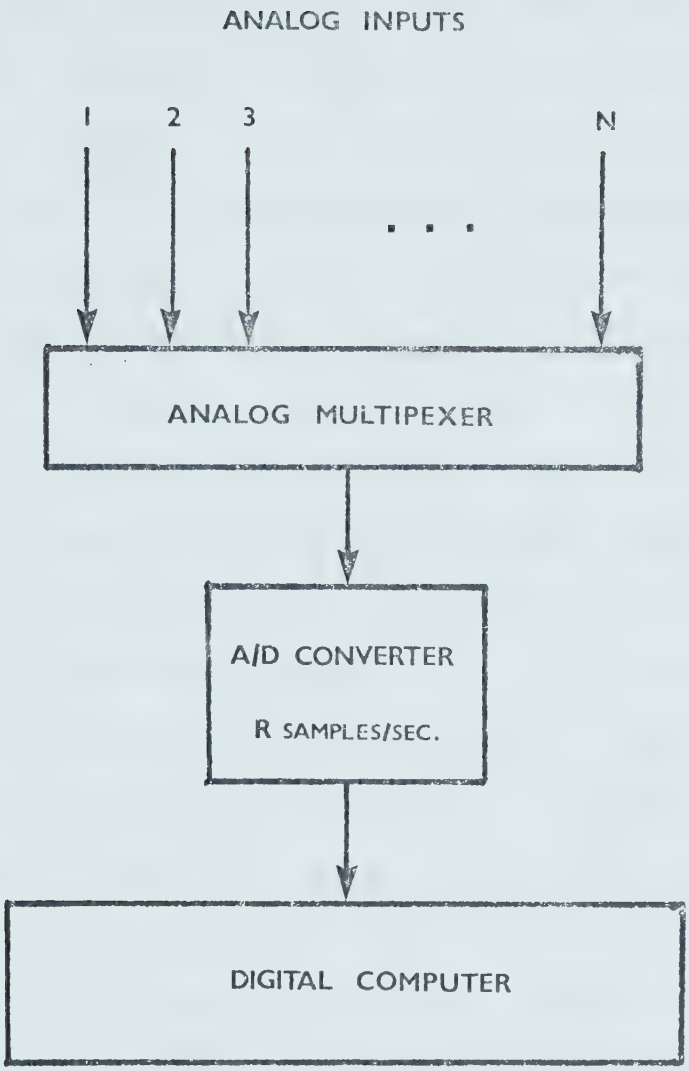


Figure 1-1 A common data acquisition system.

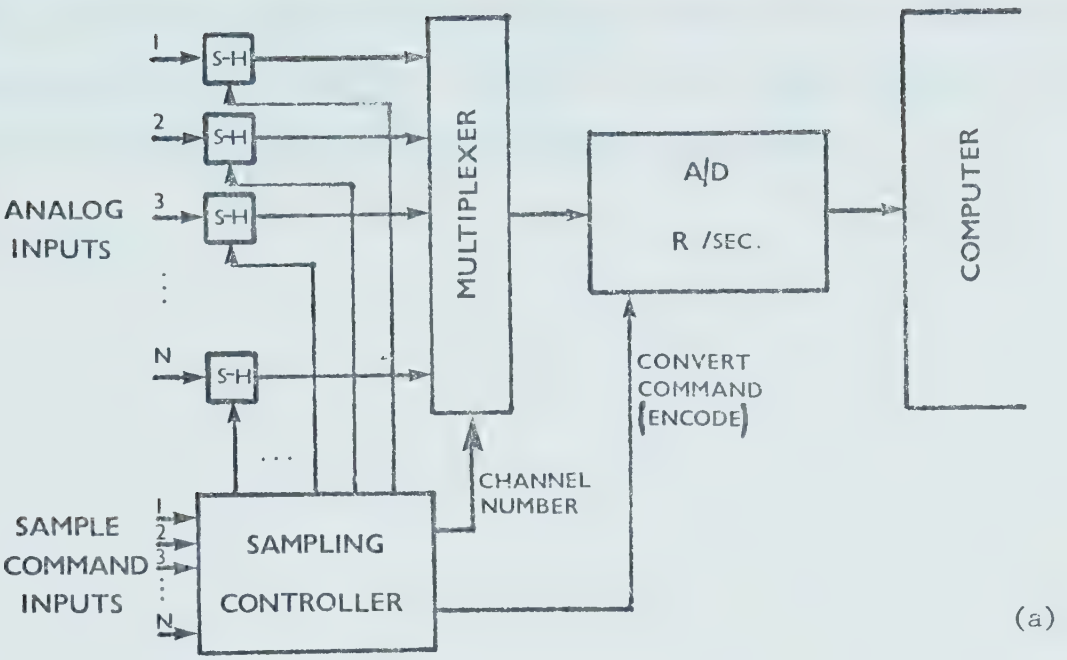
obtain the analog value of several channels at the same point in time. This problem has been overcome by connecting a sample-hold circuit on each channel before the multiplexer.[2] The sample-hold modules operate simultaneously to retain the analog value on each channel until all channels can be converted. Third, there is almost no freedom to make the sampling rate of the individual channels different from one another. In fact, in most systems all channels are sampled at the same rate. However, it would sometimes be advantageous to sample each channel independently. For example, consider the case of several analog signals: one has a large high frequency content and another does not. To sample all signals at a rate fast enough for the highest frequency signal would be computationally very time consuming due to the superfluous data taken from the low frequency channels. If, on the other hand, the sampling rate is appropriate for each signal, the amount of input data to the computer can be reduced substantially. In addition, some types of signals may have bursts of activity between which exist long periods of uninteresting quiescence. To illustrate, consider a series of neuroelectric or myoelectric action potentials. For such signals, rather than sampling at a regular rate, a detector of some type could be used to initiate sampling only during periods of activity. Action potentials from a nerve or muscle usually last less than 5 milliseconds, and tens or hundreds of milliseconds lapse between them.[3,4] A regular sampling rate of several thousand per second and considerable calculation would be necessary, in this case, to determine peak values and interpeak intervals. Instead, a peak detector and timer could be used to extract this information.

1-3 The Sampling Controller

In response to the need for a more versatile data acquisition system, the Sampling Controller for a Hewlett-Packard 5610A analog-to-digital converter was designed. The 5610A is a 16 channel multiplexed analog-to-digital converter which is interfaced to a Hewlett-Packard 2100A computer. The Sampling Controller makes an N channel converter appear like N single channel converters (Figure 1-2).

The most important feature of the Sampling Controller is that the sampling rate of each channel can be controlled independently. Each analog input on the analog-to-digital converter has a corresponding digital input on the Sampling Controller to which various pulse sources may be connected. (These pulse sources must, however, be compatible with Diode-Transistor Logic or Transistor-Transistor Logic). Every time a High to Low transition occurs at one of the digital inputs, the corresponding sample-hold circuit stores the analog value on that channel. A short time later the Sampling Controller signals the converter to sample the output of this sample-hold circuit. The rate at which a channel is sampled need not be regular, but it must remain below a certain maximum which is determined by the number of channels being used and the conversion rate of the converter. Any number of channels may be sampled simultaneously simply by connecting the respective sample command inputs to the same pulse source.

A special facility has been included in the Sampling Controller to deal with neuroelectric and myoelectric information. A digital timer allows the time intervals between the sampling pulses, occuring at any of the first four channels, to be determined. If one of the peak detectors is used in conjunction with the timer, both peak values and



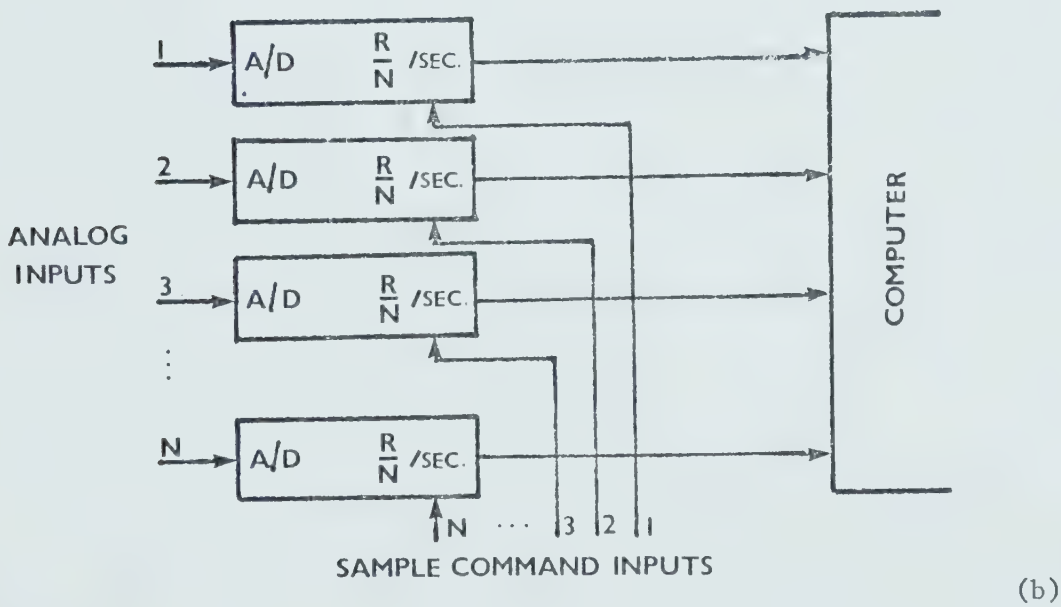


Figure 1-2 The Sampling Controller in (a), which includes the sample-hold circuits, makes the multiplexed analog-to-digital converter appear like the N separate analog-to-digital converters with reduced sampling rate in (b).

interpeak intervals may be extracted from a train of action potentials. The time information reaches the computer during the conversion of the corresponding peak voltage. The timer resolves times as short as 10 microseconds and reaches full scale after 328 seconds.

Chapter 2

THE SYSTEM

2-1 Synopsis

This chapter deals with the design of the various parts of the Sampling Controller. Each succeeding section describes a particular part, first in general terms, and then in more detail. This section is devoted to an overview of the whole data acquisition system.

The clock and control units as well as the bank of sample-hold circuits are the most important parts of the controller (Figure 2-1). The memory, timer, and peak detectors are only auxiliary units included to enhance the usefulness of the system. Clock pulses at a stable frequency are produced by the clock or oscillator to synchronize operations in various parts of the controller.

The control unit regulates the state of the analog multiplexer and initiates all conversions. When a pulse appears at a sample command input of the control, a flag is set, and a corresponding sample-hold circuit is switched from the sample mode to the hold mode. The output of the sample-hold circuit follows the voltage at its input until the mode change occurs; then the voltage is maintained until the converter is able to sample it. All flags are continually scanned at the clock frequency until a flag that has been set is detected. Upon the detection of a set flag, the control stops the scanning process, switches the analog multiplexer to the corresponding channel, and issues an encode command to the converter. After the converter has sampled the value

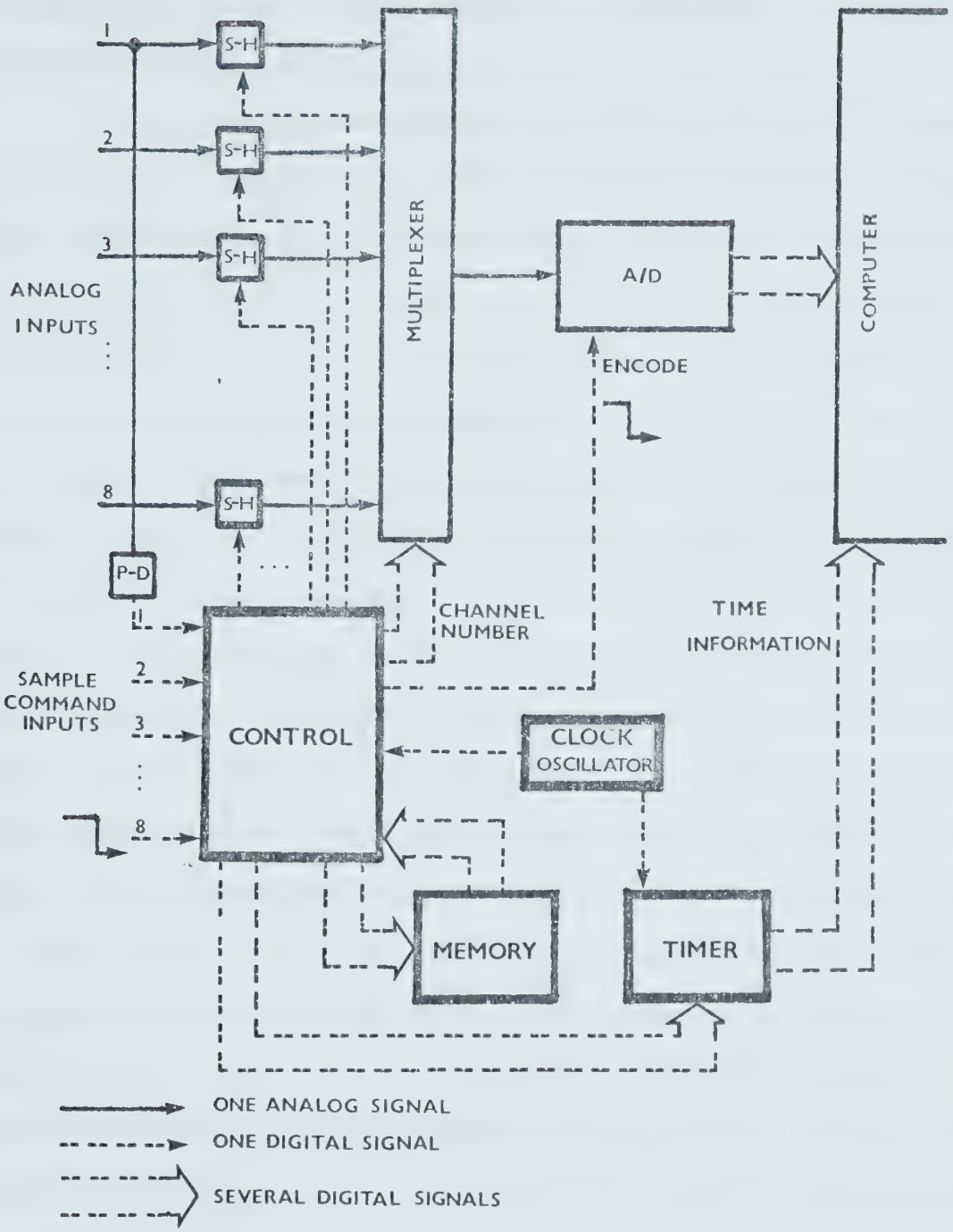


Figure 2-1 The data acquisition system including the Sampling Controller.

presented by the multiplexer, the flag in the control is cleared, and the sample-hold circuit is released from the hold mode. The scanning is resumed when the conversion is complete.

The timer is capable of measuring the time intervals between the appearance of pulses at any of the first four sample command inputs. When a pulse arrives at one of these inputs and sets the flag, the state of the timer is stored in a buffer, and the timer is reset to zero. During the time that the corresponding analog channel is converted, the information in this buffer is transferred to the computer. Four switches mounted on the front panel of the controller make it possible for all, some, or none of the first four channels to be connected to the timer. For example, if only one channel is connected to the timer, the time intervals between sampling pulses on that channel only are measured.

There is a possibility that the control may initiate conversions in a different order than the order in which pulses arrive at the sample command inputs. For instance, flags 3 and 1 may be set, in that order, but the control may cause channel 1 to be converted first. When the timer is used, this would cause the time information to be sent to the computer in the incorrect order. The purpose of the memory is to ensure that the correct order is preserved. The order of arrival of pulses at any of the first four sample command inputs is stored in the memory, and the memory acts on the control to allow conversions only in this order.

The two peak detectors included in the controller are useful in reducing the quantity of sampling required with some types of signals. A peak detector is usually connected as shown in Figure 2-1. When a peak occurs, the detector transmits a pulse to the control which signals

the correct sample-hold circuit to retain the peak voltage until conversion. The peak detector may be operated in a variety of modes which expand its usefulness.

Although only 8 sample-hold circuits have been made, the system has been built to accommodate 16 of them. In addition, the memory may be immediately expanded from 4 to 8 channels.

2-2 The Control Unit

The control logic, the oscillator, and a bank of sample-hold circuits are all that are needed for the operation of the basic system. With just these, it is possible to sample any channel at any rate below a certain maximum.

The order of events when a pulse arrives, at say sample command input 3, is as follows.

(1) The pulse sets a flag (flip-flop) corresponding to channel 3.

(2) The state of the flag determines the state of a corresponding sample-hold module which is connected to the channel 3 analog source. As soon as the flag is set the analog value at that moment is held.

(3) A divide by 16 counter with decoding gates is driven at 1.024 MHz. and interrogates each flag in turn. When the sampling pulse arrives at flag 3 the counter can be interrogating any flag from 1 to 16; but for discussion, let it be at flag 5.

(4) If no other pulses are allowed to set other flags the counter will unsuccessfully interrogate flags 5 to 16, 1, and 2 before it arrives at flag 3.

(5) The set state of flag 3 is detected and an encode pulse is sent to the analog-to-digital converter to start a conversion. Also, a mode flip-flop is set which initiates the pause phase which lasts for 11 microseconds.

(6) During the pause phase the counter is not incremented but instead switches the multiplexer on the converter to channel 3.

(7) Approximately 4 microseconds after the commencement of the conversion, flag 3 is cleared which releases the sample-hold circuit from the hold mode. (During the third microsecond after the beginning of the conversion, the analog sample is transferred to an internal sample-hold circuit in the analog-to-digital converter). Then, 11 microseconds after the beginning of the conversion, the converter resets the mode flip-flop and the scanning process resumes.

Three points should be made clear. First, a pulse is ignored if it arrives at flag 3 after it is set, but before it is cleared. This is how the control limits the sampling rate of a channel. A quantitative treatment of the maximum sampling rate is given in Appendix 1. Second, the time required by the analog-to-digital converter to digitize a voltage is 10 microseconds. The Sampling Controller allows 1 extra microsecond per conversion and takes 1 microsecond to interrogate a flag. Third, it is possible to switch the output of a chosen decoding gate back to the clear input of the counter. Fewer than 16 flags may then be scanned to avoid the unnecessary waste of time caused by interrogating flags corresponding to unused channels. This saving produces an increase in the maximum sampling rate of the active channels.

The construction of the control unit is shown in Figure 2-2.

The control can be most easily understood by considering its two modes of operation.

Scan Mode. In this mode, the scan counter runs at the 1.024 MHz. oscillator frequency. The scan counter is semi-synchronous. That is, it is neither completely a synchronous counter nor a ripple counter. Rather, it is partly both, and represents a compromise between the speed of a synchronous counter and the simplicity and lower cost of a ripple counter. The outputs of the scan counter drive the inputs of the decoding gates (D1 to D16). The counter-decoding gate arrangement assures that one and only one flag is interrogated at a time.

The decoding gates D1 to D8 have an extra input which may be controlled by the memory. Only gates D1, D2, D3, and D4 are actually connected to the memory however, because only a four channel memory has been built. The function of a decoding gate is three fold. First, a particular gate DN (where N=1,2,3,...,16) with a gate QN allows only flag N to be detected. Secondly gate DN along with gate SN assures that only flag N is cleared after channel N is converted. And finally, a switch is provided to allow the output of a particular gate DN to be connected to the clear inputs of the scan counter so that only the first N-1 flags are scanned.

If a flag N is set, and if the scan counter activates gate DN, a level change ripples through gate QN and the 16 input gate C. The clock pulse CP2 is suitably delayed from CP1 to allow for adequate settling time before relaying the level change at gate C to the mode flip-flop. When CP2 does appear at gate E the mode flip-flop is immediately toggled, and a one-shot multivibrator sends an encode pulse to the analog-to-digital converter. The encode pulse initiates a

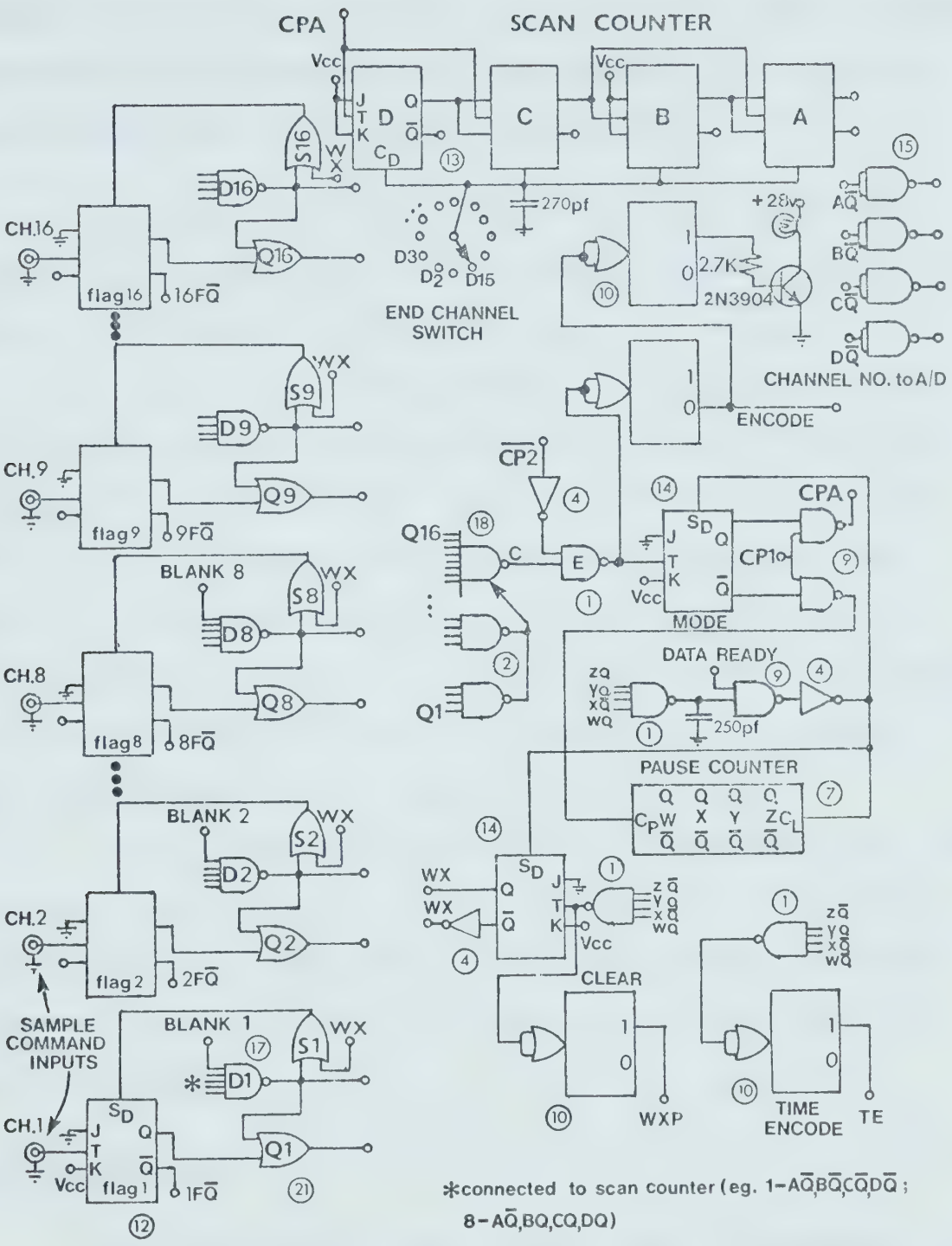


Figure 2-2 The control unit. (The circled numbers indicate logic function - see Appendix 2.)

conversion, and the buffered outputs of the scan counter switch the multiplexer to the correct channel. At the same time, another monostable multivibrator blinks a panel mounted lamp to indicate that an encode pulse is being sent. The pause mode is now entered.

Pause mode. The mode flip-flop, when toggled to the pause state, stops the flow of clock pulses to the scan counter, and instead directs them to the pause counter. The function of the pause counter is to determine the order and timing of events in the pause mode. The clear flip-flop, after 4 microseconds in the pause mode, changes state and clears the appropriate flag. That flag is held in the clear state until the end of the pause mode to allow the associated sample-hold circuit time to acquire the new signal. The clear monostable multivibrator advances the memory if it is in use (see Section 2-3). Another monostable multivibrator (time encode) sends a pulse to the computer to load time information into the computer interface.

The pause mode may be terminated by a (data ready) pulse from the analog-to-digital converter or by the pause counter after 11 microseconds have elapsed. When either of these things happen, the pause counter, the clear flip-flop, and the mode flip-flop are cleared and scanning is resumed.

2-3 The Memory Unit

If only the control logic is used, there is no assurance that the channels will be converted in the same order as the order in which sampling pulses arrive at the sample command inputs. A set flag indicates only that a pulse arrived some time in the past, but indicates nothing about the time that the flag was set with respect to the others.

The scan counter interrogates the flags in numerical order so that the channels are converted in that order, regardless of the order in which they are set. When the timer is used it is essential that the time information be sent to the computer in the proper order. Some type of memory is therefore necessary for use with the timer.

Channels one through four only are associated with the memory. Switches corresponding to each of the first four channels are provided on the front panel so that any combination of them may be put under memory control. For example, if switches two and three are turned on, channels two and three will always be converted in the same order as their flags are set.

The type of memory used in the Sampling Controller is shown in block form in Figure 2-3. It is a two dimensional array of flip-flops. One co-ordinate of the array is the priority level and the other is the channel number. Priority level A is the highest and indicates to the control which channel of the four should be sampled next.

A typical example of the time sequence of operation follows.

(1) A pulse sets flag 2 which results in the setting of bit A2 in memory (assuming that the memory is initially clear).

(2) When the control next checks on the state of flag 2, it finds that it is set, so a conversion is initiated. As flag 2 is cleared, the memory is shifted to the left which effectively clears it.

(3) Now, let flags 2 and 1 be set in rapid succession, in that order. Memory bit A2 is set. Then, since priority level A is occupied, bit B1 is set.

(4) The control, on its next scan past the first four flags, does

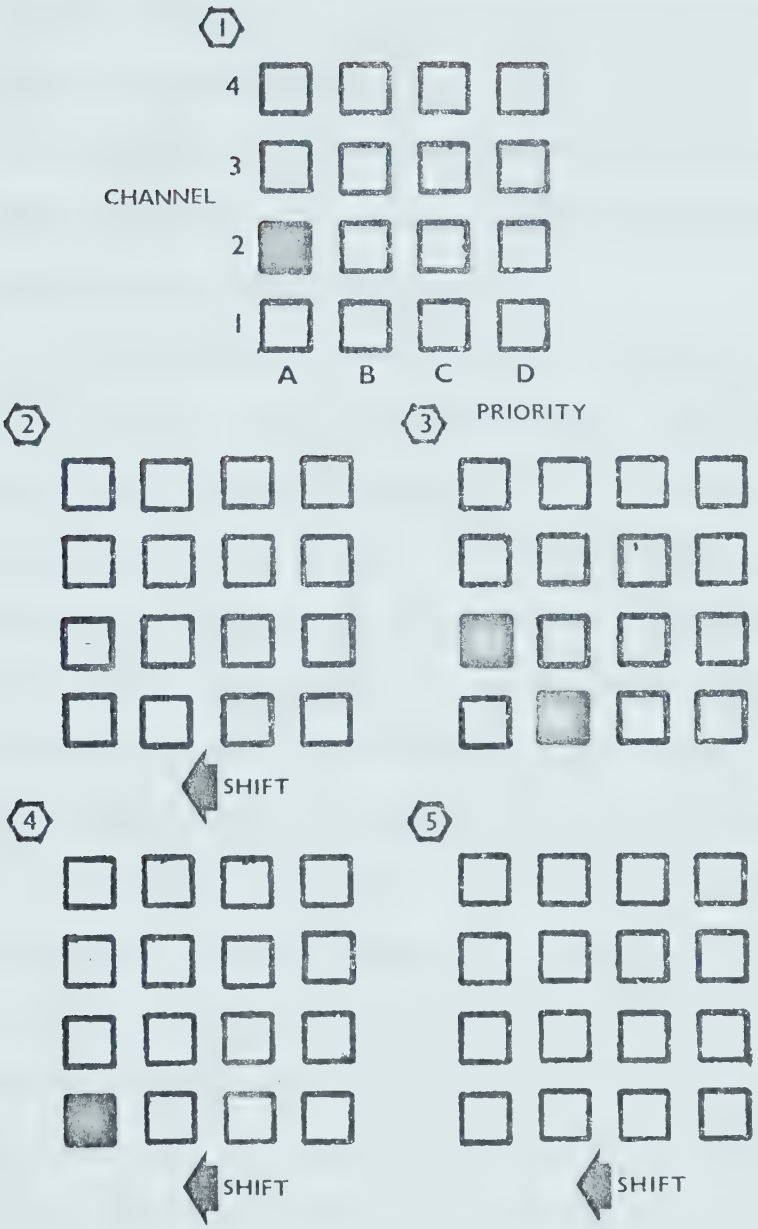


Figure 2-3 Memory operation.

not detect the set state of flag 1 because the memory masks it. Flag 2, however, is detected and cleared so that the memory is shifted to the left which places channel 1 in the highest priority level.

(5) After another complete cycle the control arrives again at flag 1 which is now unmasked. Channel 1 is converted and another shift clears the memory.

It can easily be seen that the number of bits in the memory increases as the square of the number of channels under memory control. Also, expansion of the memory is difficult because it must be expanded in two directions with an associated increase in logic complexity. These problems can be partly overcome by having two levels of memory. Smaller blocks of (4x4) sub-memory are controlled by a master memory. The sub-memories store the relative order in which four flags are set and the master memory stores the order in which the sub-memories accept information. For example, if flags 4, 6, 3, and 1 are set in that order, the first sub-memory, which is associated with flags 1 to 4, stores the order in which flags 4, 3, and 1 are set, and the second sub-memory, which is associated with flags 5 to 8, stores the fact that flag 6 is set. At the same time, the master memory records the order in which the sub-memories should be enabled and disabled. That is, since flag 4 is set first, sub-memory #1 has the highest priority and is enabled first. Flag 6 is set next, so sub-memory #2 has the next highest priority. Sub-memory #1 is given the third and fourth priority for flags 3 and 1. With two levels of memory, expansion is accomplished by adding more blocks of sub-memory and changing the master memory.

The number of bits required by the two levels is not as great as that required by one large block of memory. For eight channels, 64 (8x8) bits are required if one block of memory is used. When two (4x4) sub-memories, and one (2x8) master memory are used instead, the total quantity of memory bits is reduced to 48.

The remainder of this section explains the design of the memory in greater detail.

Sub-Memory. The sub-memory, shown in Figure 2-4, is associated with the first four channels. (Provision is made for the addition of another sub-memory for channels 5 to 8). Switches A, B, C, and D allow channels 1, 2, 3, and 4 respectively to be subjected to memory control. An example of how information is entered into, and erased out of the sub-memory follows. At first, assume that all four switches are on. That is, A, B, C, and D are connected to a 5 volt supply through the 100,000 ohm resistor. In addition, let the memory be initially clear.

If flag 2 is set, an altered output $2F\overline{Q}$ from this flag appears at the input of a latch. The pulse train CPS loads the new flag level into the latch so that $2F\overline{Q}$ is presented at the input of gate G2. Some time later a strobe pulse (produced by the strobe counter shown in Figure 2-5) causes the output of G2 to change momentarily. Since the memory is clear, S2A transmits this pulse to the set input of flip-flop 2A. The presence of a set flip-flop in a previously clear row, activates gate P2, which inhibits gate G2 so that it cannot set another flip-flop until the row is cleared by a shift.

The purpose of the strobe counter is to eliminate racing for one priority level in the memory, but it has one important disadvantage;

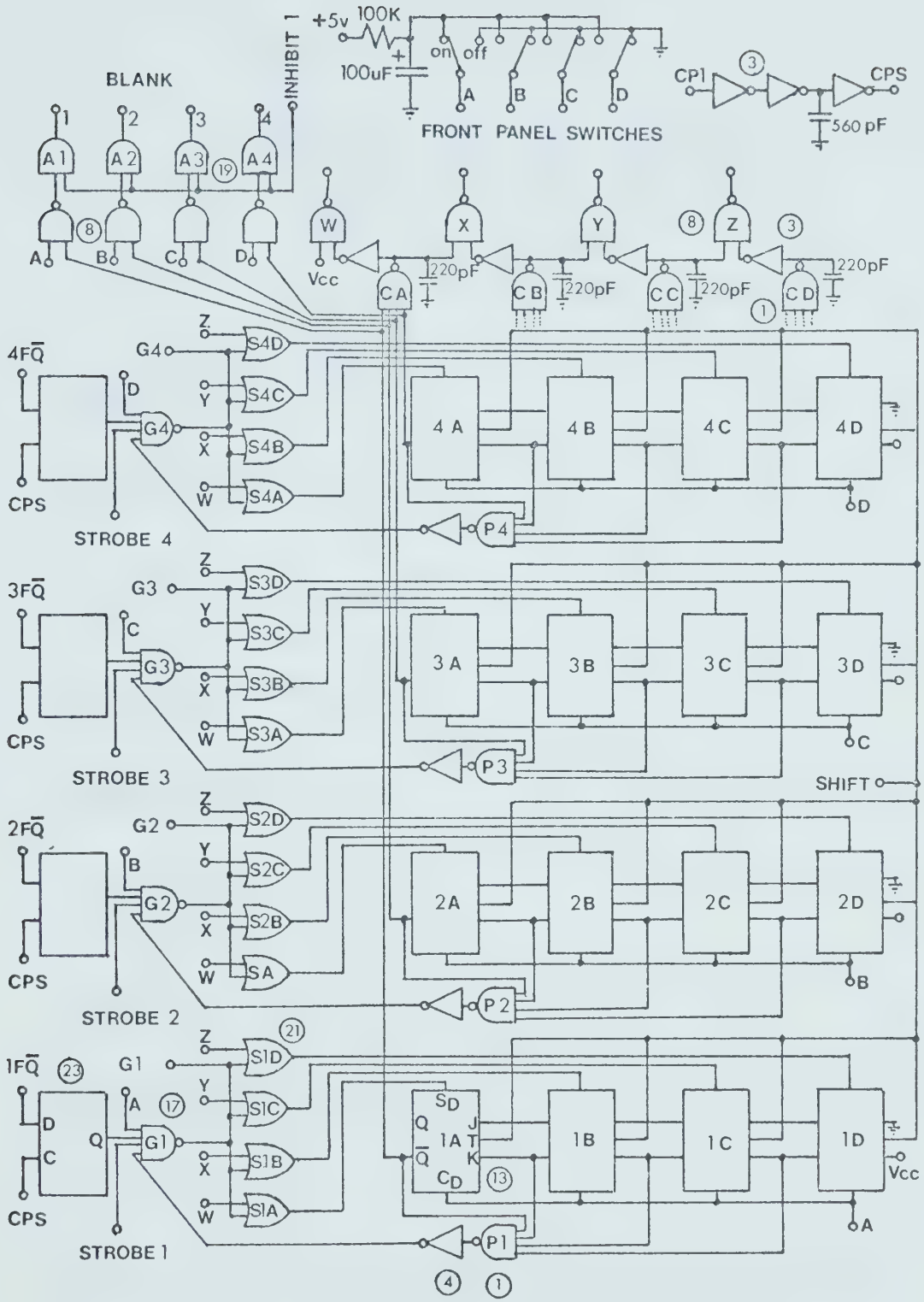


Figure 2-4 The sub-memory. (The circled numbers indicate logic function - see Appendix 2.)

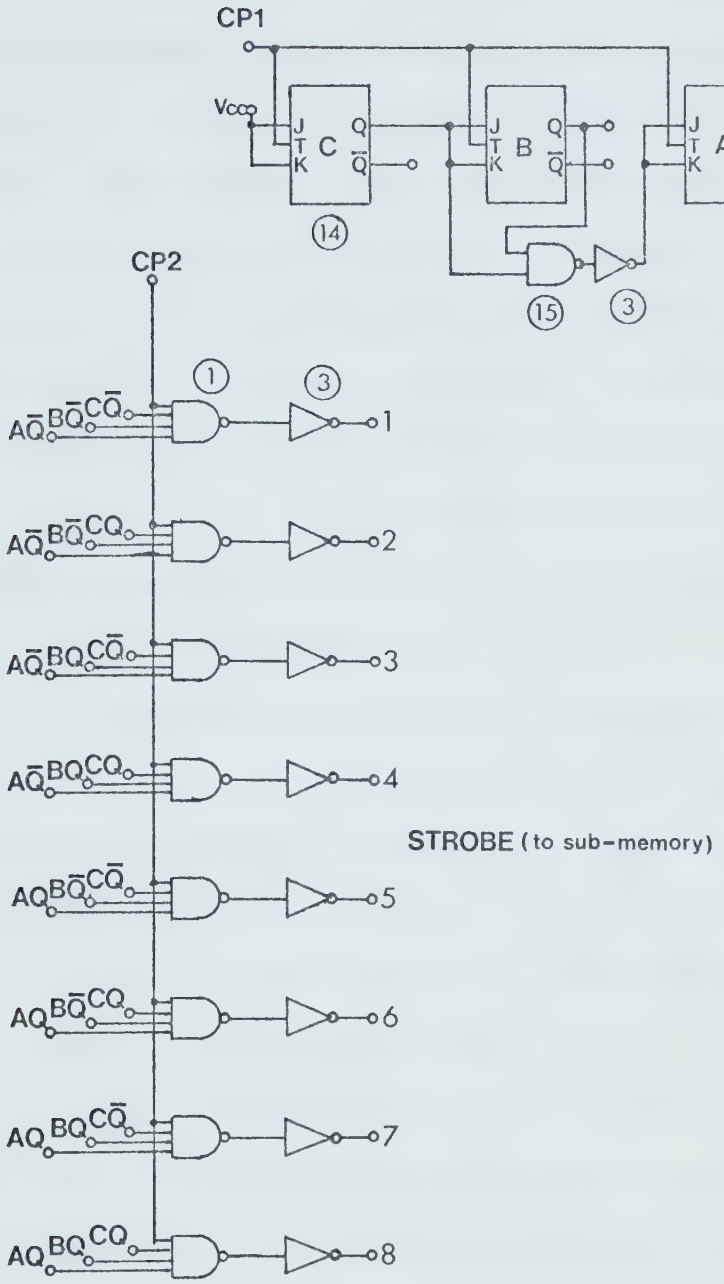


Figure 2-5 The strobe counter and decoding gate assembly for the sub-memory. Note: $A\overline{Q}$ is wired to V_{CC} rather than the counter because only one sub-memory has been made. Therefore, the cycle time is reduced from 8 to 4 microseconds.

it limits how well order can be discriminated at short time intervals. If, for instance, flags 1, 3, and 2 are set in that order, less than 8 microseconds apart, they will not be entered into the memory in that order, but in the order in which the strobe counter pulses the G series of gates. Flags set more than 8 microseconds apart, however, are properly discriminated. Since only one sub-memory has been made, the strobe counter and decoding gate assembly has been modified to have a cycle time of 4 microseconds rather than 8 microseconds.

A network of gates determines which flip-flop in the memory is set. Gates CA, CB, CC, and CD along with gates W, X, Y, and Z select the column of highest priority which is not occupied. The S series of gates select the appropriate row.

The way in which the memory influences the control is as follows. The output of each flip-flop in the highest priority column (A) is connected through two gates to an input of a corresponding gate DN (N= 1, 2, 3, 4) in the control. Only one flip-flop can be set in column A at any one time so only the corresponding flag can be detected by the control; all others are masked.

When a flag is detected by the control, the pause phase is begun, during which the flag is cleared and a monostable multivibrator sends a pulse (WXP) to the shift logic shown in Figure 2-6. The shift logic ensures that a conversion of only those channels which are switched on initiates a shift. Since each row of the memory is simply a shift register, pulse WXP shifts all information one column to the left, with nulls appearing in column D.

It is worthwhile to examine the functions of the switches more closely. When the power is turned on, problems would arise if the

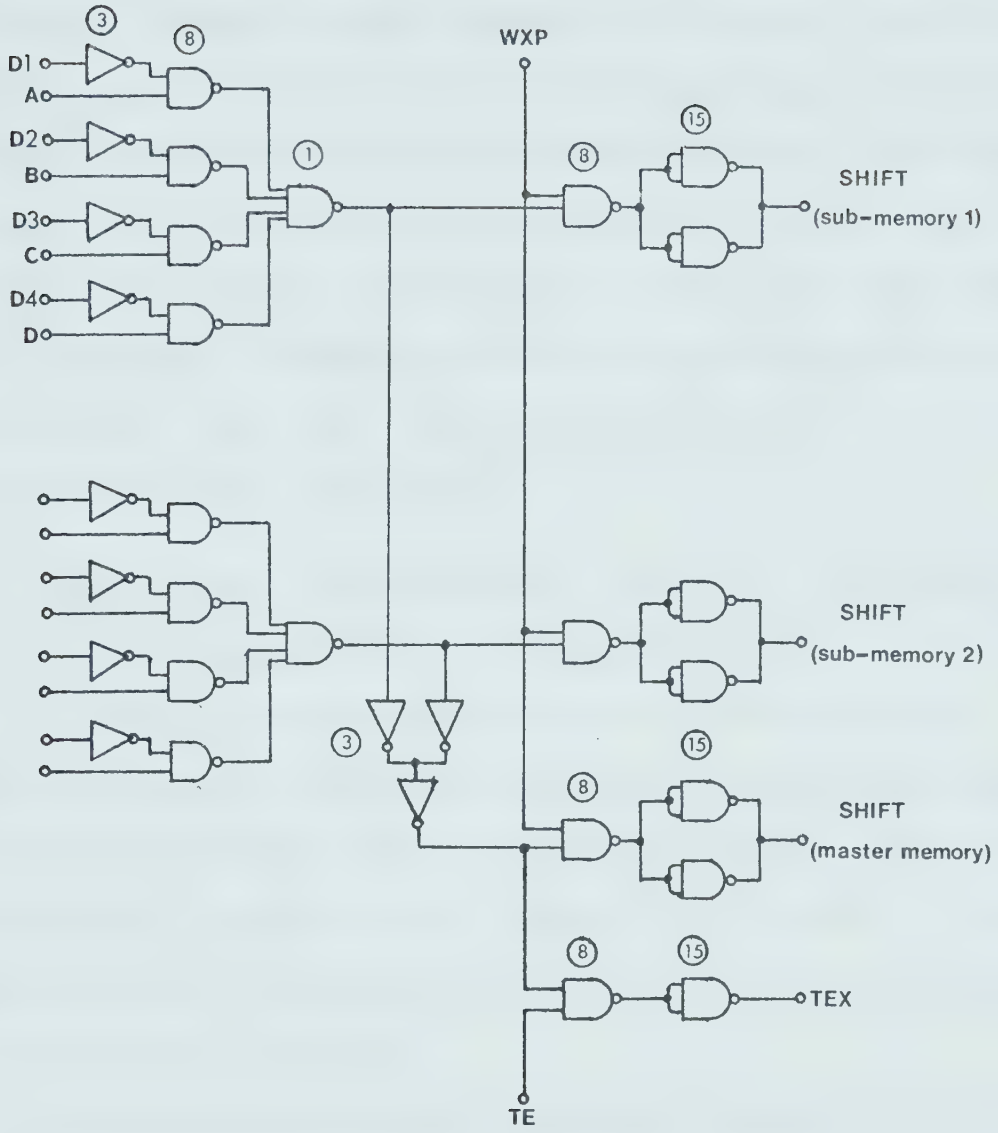


Figure 2-6 The shift logic.

flip-flops in the memory were allowed to assume a state randomly. More than one flip-flop could be set in a particular row or column, or worse still, a place in the memory could be set with no corresponding set flag in the control. A simple resistor-capacitor circuit solves this problem. If a switch happens to be in the on position during turn on, the 100,000 ohm resistor and 100 microfarad capacitor hold the clear inputs of the corresponding row of flip-flops low, long enough to clear that row. If a switch happens to be off, the clear inputs of that row of flip-flops are held low anyway. Furthermore, the switches are used elsewhere in the sub-memory and shift logic to allow only channels that are on to use the memory and affect the control.

Master Memory. The master memory (Figure 2-7) is intended to control the order of operation of two sub-memories like that shown in Figure 2-4. In the master memory there are two rows of flip-flops corresponding to the two sub-memories, and eight columns corresponding to the eight total priority levels of the two sub-memories. When any of the four gates G1 to G4 (or G5 to G8) transmit a pulse to write in the sub-memory, this pulse also writes in the master memory. The logic at the top of Figure 2-7 does this.

In most respects the master memory and sub-memory are similar except for one important difference; more than one flip-flop can be set in either row of the master memory. In fact, up to four can be set in either row. Every time either sub-memory is shifted, the master memory is also shifted by the logic shown in Figure 2-6. This action masks and unmasks the sub-memories in proper sequence. Flip-flops 1A and 2A are connected to gates A1, A2, A3, and A4 in both sub-memories (Figure 2-4). Therefore, the state of these flip-flops can inhibit the

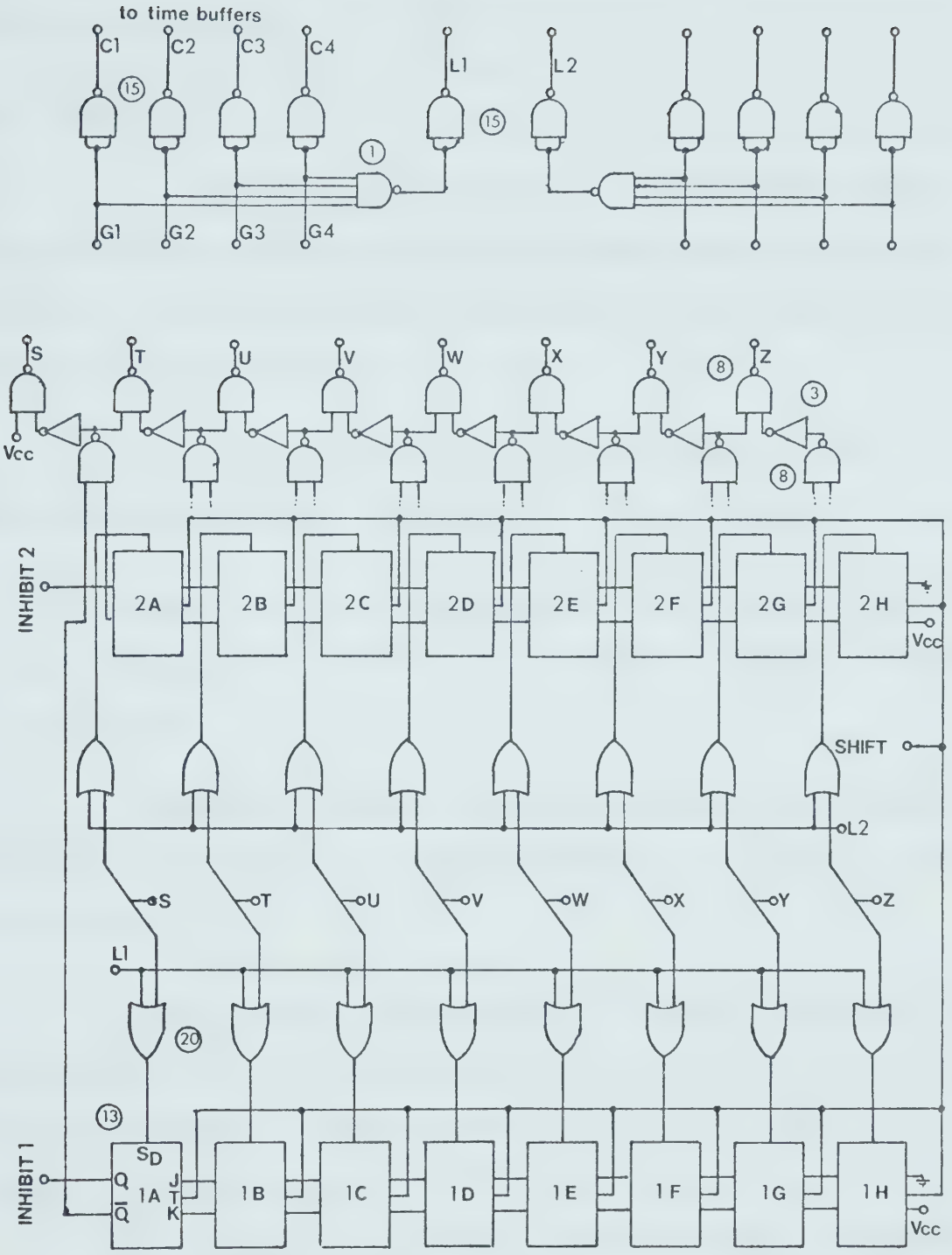


Figure 2-7 The master memory.

blanking lines from the sub-memory to the control, thereby performing this masking function.

2-4 The Timer

The main motivation for including a timer in the Sampling Controller is to measure time intervals between peaks of myoelectric spikes. To do this and operate effectively the timer must fulfil the following requirements.

Great Range. The timer should resolve small fractions of milliseconds and yet have a full scale of at least several minutes.

Binary. To minimize manipulation by the computer, the timer should "speak the same language" as the computer. That is, it should be a binary timer.

Word Size. Since the allowable word size of the computer interface is 14 bits, this limitation must apply to the output word size of the timer.

Output Buffers. The operation of the timer and computer are not synchronous so storage buffers for the time information are needed. The buffers perform the same function for the digital time data as the sample-hold circuits perform for the analog signals.

The first three requirements combine to produce an interesting restriction. If a simple binary counter is used for the timer and a 10 microsecond to 100 second range is required, the counter needs to be about 24 bits long. It is obvious then, in view of the 14 bit interface restriction, that the timer cannot maintain full resolution over the

entire range. It is important, however, that as much resolution as possible be kept in the measurement of short times. A counter that provides a solution is one that automatically changes ranges.

The output word of the timer is in the form of a 10 digit binary number and a four digit binary exponent. The number .1000000000 0001 is the benchmark and is equal to 10 milliseconds. Other examples are; .1000000000 0010 is 20 milliseconds and .1100000000 0010 is 30 milliseconds. The time can be easily calculated by using the formula:

$$\text{Time} = N \times 2^{E} \times 10 \text{ milliseconds},$$

where N is the decimal equivalent of the 10 digit number and E is the decimal equivalent of the 4 digit exponent. The shortest range is 10 milliseconds and the longest is 328 seconds. The resolution of each range is 1 in 1024.

An analogy to the timer is a multirange voltmeter driven by a linear voltage ramp (Figure 2-8). At time zero, the voltmeter indicates zero volts and is on the most sensitive range. After a short time the voltmeter reaches full scale, at which time the operator moves the range switch to the next less sensitive range. Most voltmeters have decade ranges, but for the sake of similarity, let each range be only half as sensitive as the last. Therefore, upon switching ranges, the voltmeter needle drops back to half scale and continues its linear climb to full scale, but at only half the previous rate. At full scale the sensitivity is reduced once more, and so on, until the last range is reached. The reading on the scale of the voltmeter, of course, corresponds to the 10 bit binary number of the timer, and the range switch serves the same function as the four digit exponent.

The operation of the timer with respect to the rest of the

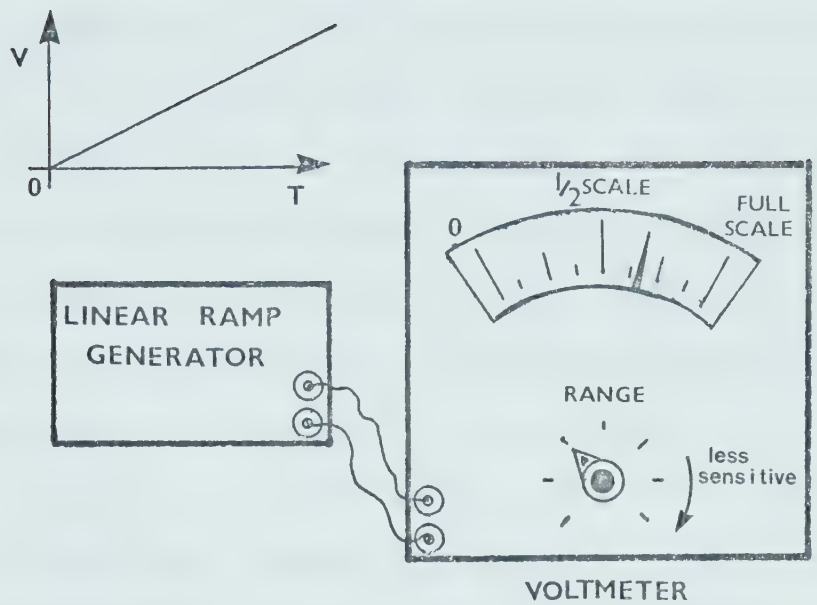


Figure 2-8 Voltmeter analogy to timer.

the first four channels, three things happen almost simultaneously. That channel is ranked in the memory according to arrival order, the time information is loaded into a buffer, and the timer is reset to zero. Later, when that channel is being converted, the time information stored in the buffer is transmitted directly to the computer interface.

Furthermore, the timer can be influenced by two front panel controls: a button, and a switch. The RESTART button, when pressed, resets the timer to zero. The three-position END SCALE switch stops the timer at three different times (1.28 sec., 10.2 sec., and 328 sec.). After the timer runs for the length of time indicated by this switch, a blue lamp comes on and the value of the timer becomes .1111111111 1111. The timer stays at this value until reset to zero.

The two part construction of the timer is depicted in Figures 2-9 and 2-10. One part is a particular type of counter and the other part scales the clock pulse rate for that counter. The counter is separated into two parts; a divide by 1024 counter, and a divide by 16 counter. The four bit divide by sixteen counter yields the exponent.

If both the scaler and counter are assumed to be clear at first, it takes 1024 pulses at CP0 to fill up the 10 bit counter. However, when the most significant bit of the counter (flip-flop #5) goes from a 1 to 0 state, a monostable multivibrator is fired doing three things; bit 5 is reset to a 1 again, the four bit exponent counter is incremented, and the scaler is cleared. The output of the exponent counter with the sixteen NAND gates in the scaler, select a clock pulse rate that is half as fast as the previous rate. This is accomplished by simply gating the output of the next flip-flop in the long ripple counter of the scaler. This continues until both the

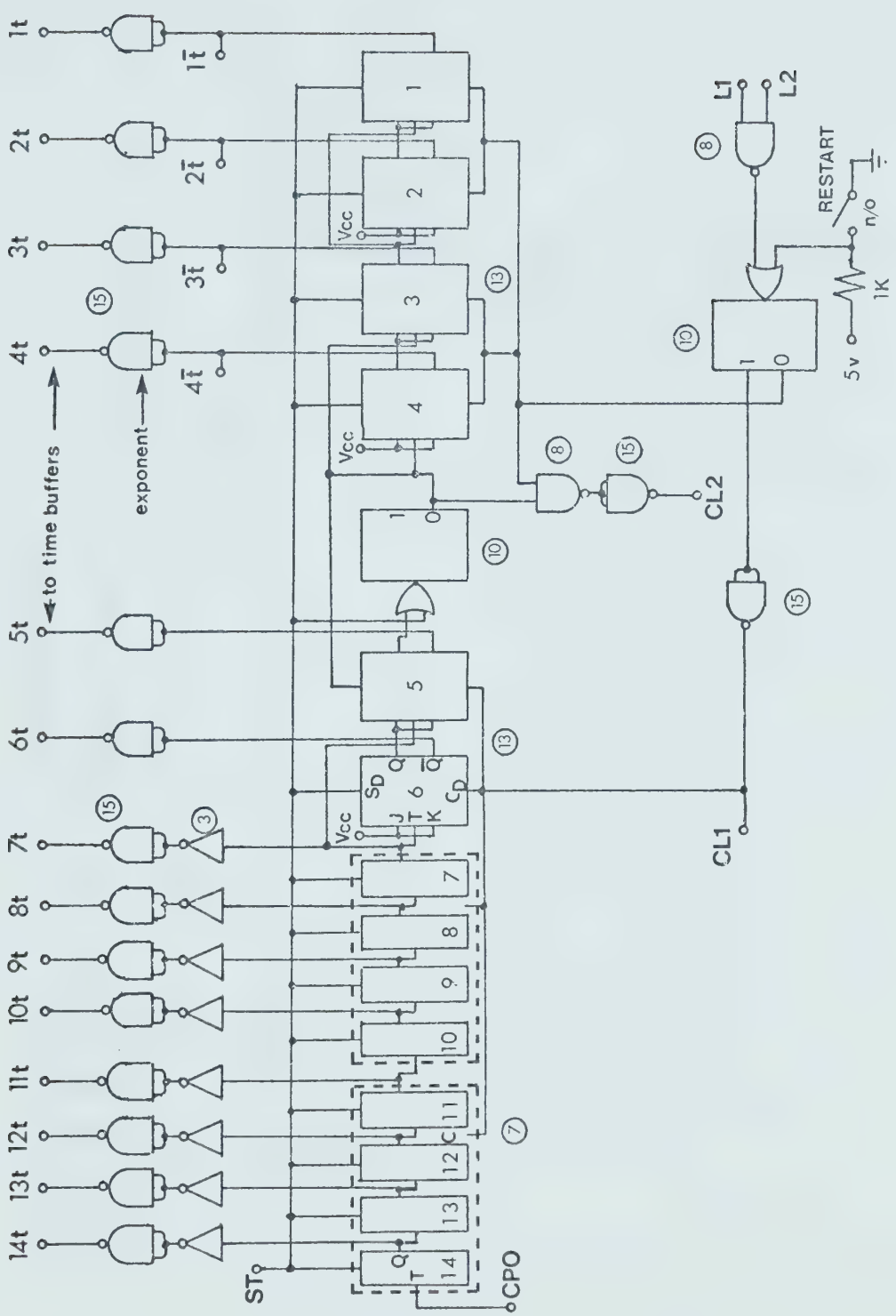


Figure 2-9 The timer (counter section). (The circled numbers indicate logic function - see Appendix 2.)

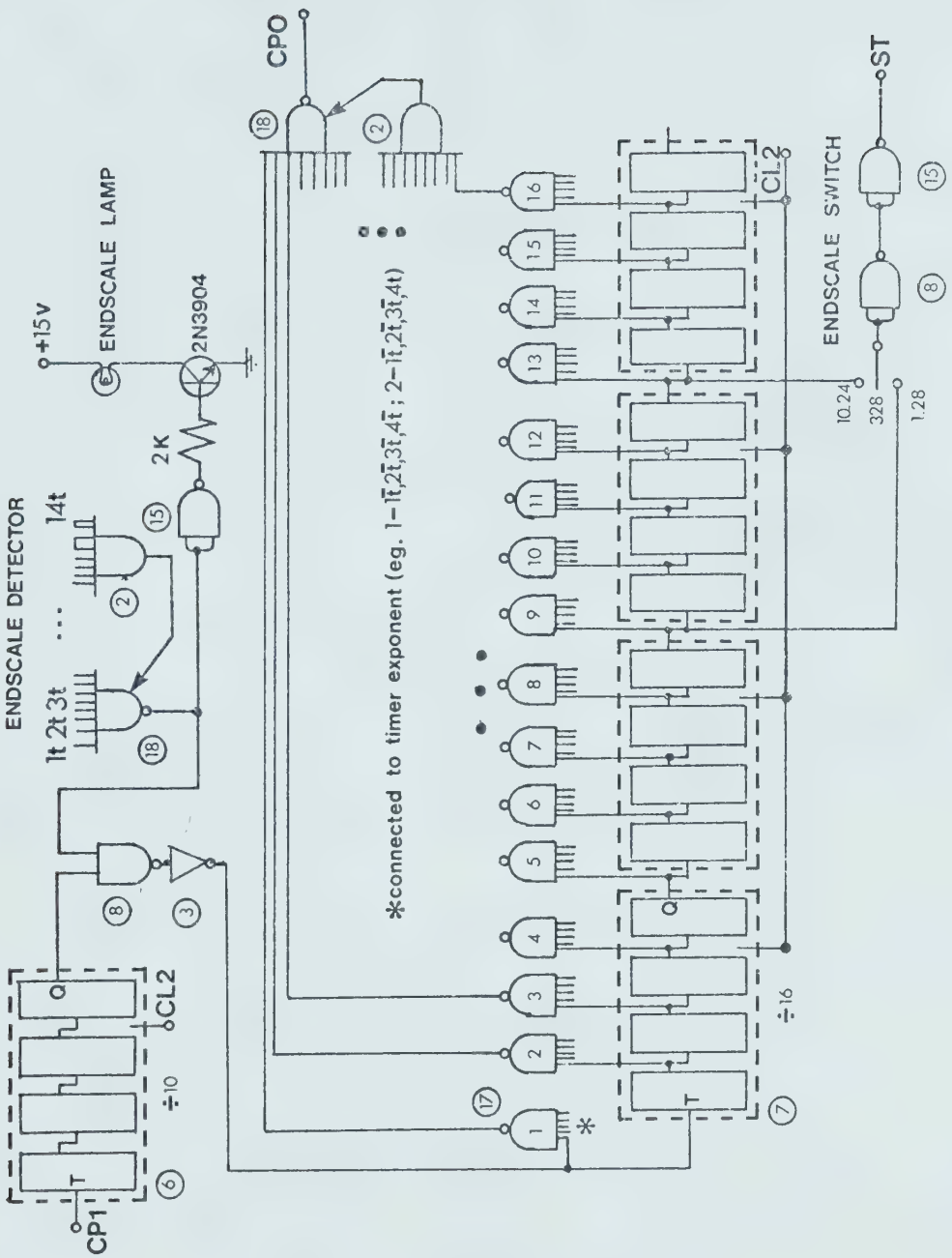


Figure 2-10 The timer (clock pulse scaler section).

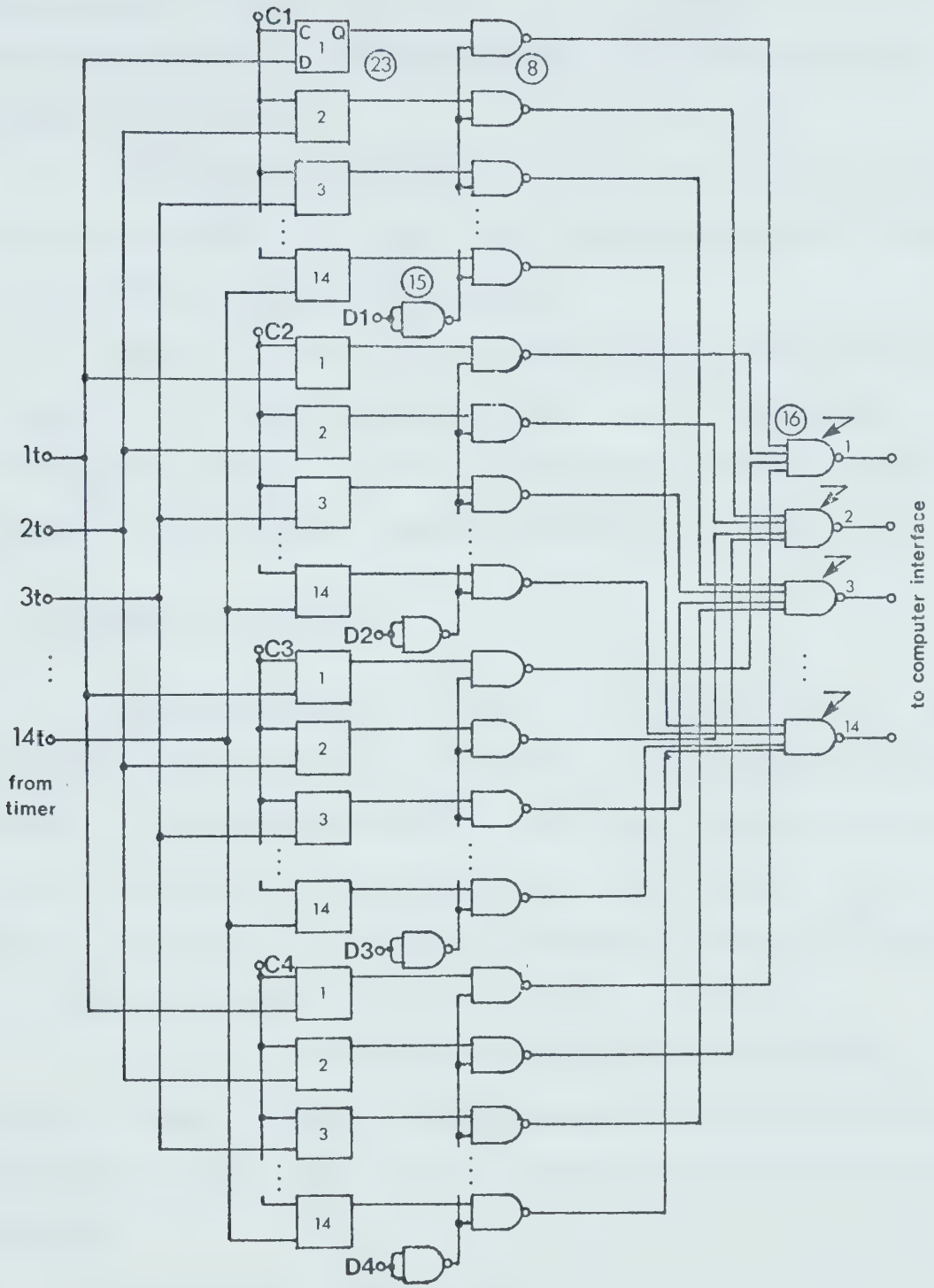


Figure 2-11 The timer buffers.

exponent counter and the ten bit counter are completely full. A fourteen input NAND gate detects this fact and inhibits the flow of clock pulses to the scaler (and therefore to the counter), and the END SCALE lamp turns on.

The restart circuit is only a monostable multivibrator which clears both the counter and scaler. The multivibrator can be fired by the manual RESTART button or by the memory.

Figure 2-11 shows the time buffers that are associated with the timer. Pulses from the sub-memory load the time information into the appropriate string of latches, and the gates multiplex the four strings of latches into the computer interface.

2-5 The Sample-Hold Module

The sample-hold module, because it is an hybrid circuit, has many specifications. That is, it is partly analog and partly digital in nature. The many compromises that can be made between the characteristics of the two modes has resulted in the great variety of sample-hold modules on the market. Some types are superior for certain applications but no single design can be used universally.

The type of sample-hold circuit used in the controller is depicted in Figure (2-12a). The basic circuit of a capacitor and switch is improved by adding input and output buffering amplifiers, each with a gain of one.

The following paragraphs deal with some limitations of practical sample-hold circuits and specific problems encountered in this application.

Aperture Time. The propagation delay of the switch and

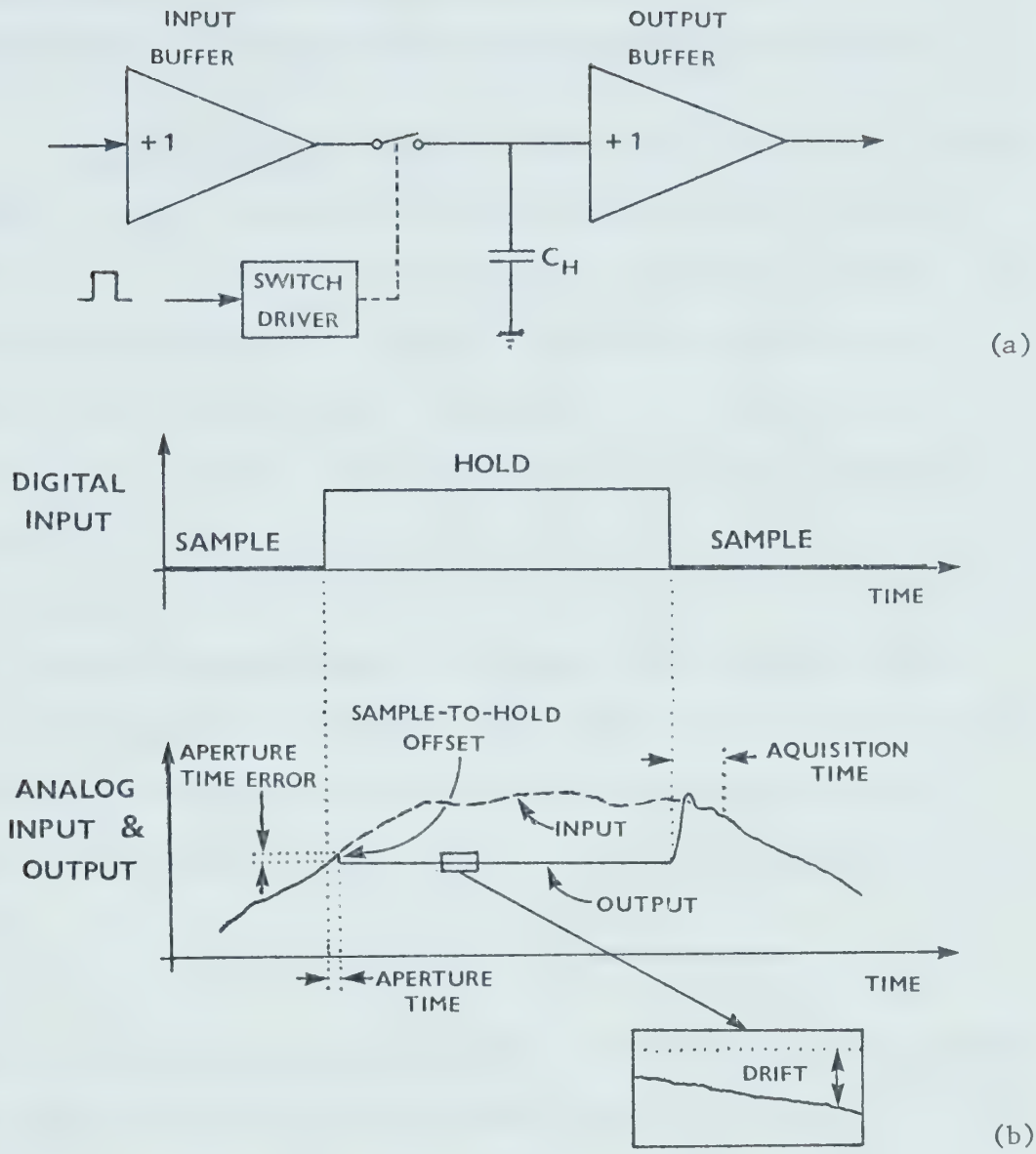


Figure 2-12 The sample-hold circuit (a), and its limitations (b).

associated logic gates allow the input signal to change before holding an analog value. Using FET switches the delay is less than 200 nanoseconds and so is not significant for most physiological signals.

Acquisition Time. When the mode changes from hold to sample, the capacitor must be charged up to the present value of the input voltage. The slew rate and settling time of the output amplifier, the output current capability of the input amplifier, and the RC time constant of the switch-capacitor combination all limit the time in which this can be accomplished. The worst case occurs when the capacitor must be charged over the full scale. The time required to do this is regarded as the acquisition time. The total voltage range in this case is ± 2.5 volts, and only 6 microseconds are allowed by the analog-to-digital converter to acquire a new signal. If a capacitor of 3 nanofarads is chosen, and if the resistance of the switch is 200 ohms the time required to reach 0.1% of the final value for an RC circuit is 9RC or

$$9(200)\ (3 \times 10^{-9}) = 5.4 \text{ microseconds.}$$

Therefore the value of 3 nanofarads for the holding capacitor is just small enough to satisfy the acquisition time restrictions.

Drift in Hold. Leakage currents from three main sources cause the holding capacitor to discharge in the hold mode. $I_{Leakage}$ may be composed of the input bias, and leakage current of the amplifier; the leakage current of the capacitor, and physical circuit arrangement; and the leakage of the switch. The discharge rate of the capacitor may be expressed as

$$\frac{dV}{dt} = \frac{I_{Leakage}}{C} .$$

The maximum time that a sample must be held may be found by the formula presented in Appendix 1, with M = 8 and N = 16. A value of 0.89 milliseconds results, but for a conservative design, 1 millisecond is taken as the length of time that the drift must remain well within the resolution of the analog-to-digital converter. Using this, a simple calculation yields:

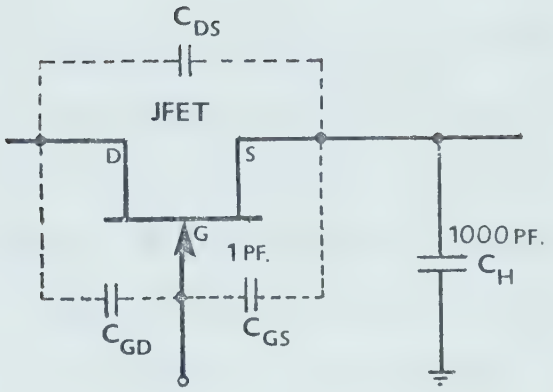
$$I_{Leakage} < \frac{\Delta V}{\Delta t} C = \frac{2.5 \text{ mv.}}{1.0 \text{ ms.}} \quad (1.0 \text{ nf.}) = 2.5 \text{ na.}$$

Therefore, if the holding capacitor is 1nf., $I_{Leakage}$ must be less than 2.5 na. A FET input amplifier at the output, a low leakage switch, and a low leakage holding capacitor are therefore required.

Sample-to-Hold Offset and Feedthrough. Capacitances in the switch subtract a small amount of charge from the holding capacitor when the module is switched from sample to hold. If the gate of the FET switch is driven through 15 volts and if C_{GS} is reasonably assumed to be 1 pf., the voltage offset for a 1 nf. holding capacitor is 15 mv. (Figure 2-13). But the resolution of the analog-to-digital converter is about 5 mv., so this error is intolerable. This problem may be solved by adjusting the offset of the output or input amplifier to compensate for this effect, and keeping C_H as large as possible to minimize it.

Feedthrough occurs when an attenuated version of the input signal appears at the output of the module when it is in hold. The switch capacitance C_{DS} is the offender in this case. However, if C_H is made large, the problem is minimized.

Voltage Gain and Gain Accuracy. If a voltage follower configuration is used for both input and output buffers, a gain of very



$$\Delta V_{C_{GS}} C_{GS} = \Delta V_S C_H$$

$$\frac{15v \times 1pF}{1000pF} = \Delta V_S = 15mv$$

Figure 2-13 The origin of the sample-to-hold offset error.

close to unity is assured. The gain nonlinearity is less than 0.01% if both common-mode rejection ratio and open loop gain of the operational amplifier are larger than 80 db.[5] Therefore the voltage follower is easy to use and maintain because gain adjustments or calibrations are never necessary.

Temperature Stability. Temperature profoundly affects the magnitude of the input bias current of the FET input operational amplifier as well as the leakage current of the switch. In fact, for every 10°C rise in temperature these quantities double.[5] The size of the storage capacitor must therefore be chosen so that, even over the entire temperature range, the drift in the hold mode is not larger than the resolution of the analog-to-digital converter.

The D.C. offset of the module must not vary more than the resolution of the analog-to-digital converter. This is particularly difficult to achieve with a FET input operational amplifier. Modern FET amplifiers are temperature compensated, and offset trimmed by a laser.[6] However, for these amplifiers, the near zero temperature coefficient is made to occur at zero offset voltage. In this application, an offset voltage of tens of millivolts is needed to eliminate the sample to hold offset error. This problem is solved by using FET preamplifiers which allow an adjustment of both temperature coefficient, and offset voltage.

The circuit diagram of the sample-hold module is shown in Figure 2-14. The input and output buffers are just voltage followers, but the output buffer is composed of two integrated circuits. The FET input preamplifier (HA 2005) provides the general purpose operational

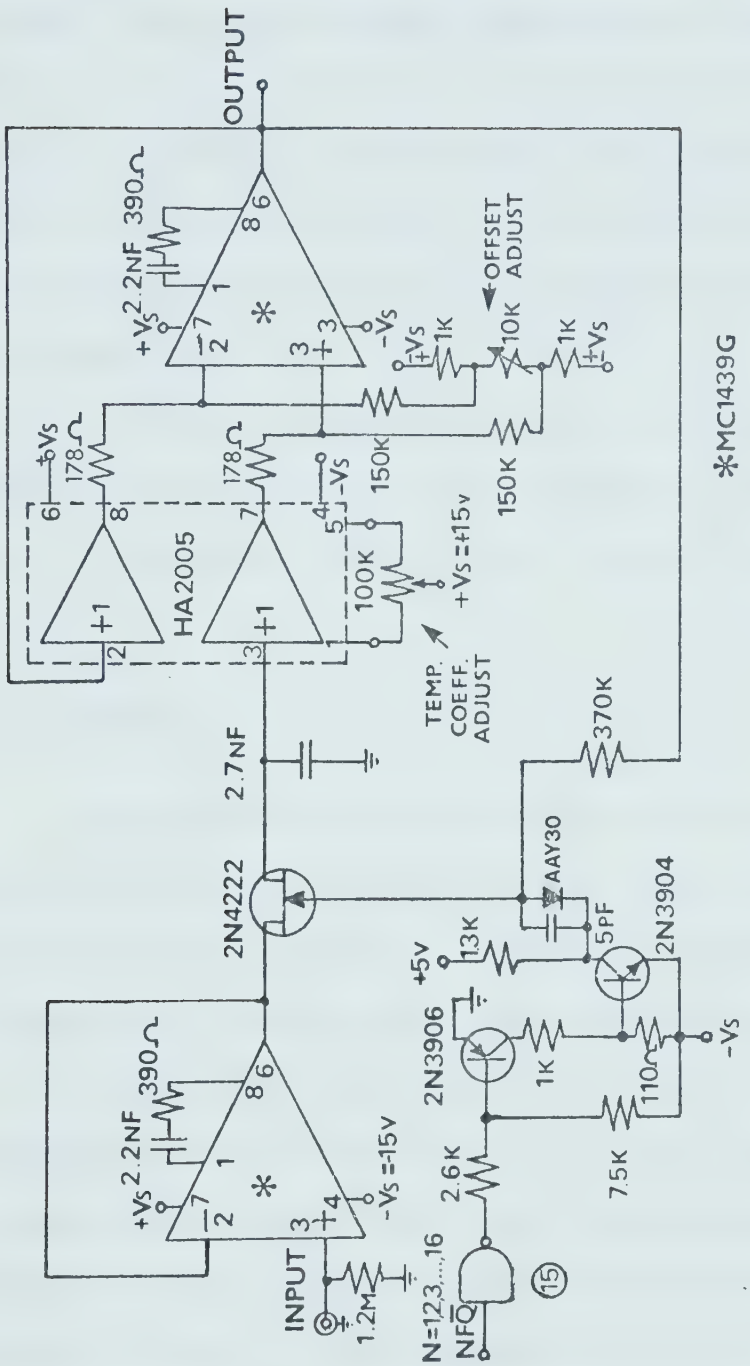


Figure 2-14 The sample-hold circuit.

amplifier, (MG1439G), with a high input impedence (10^{12} ohms), and a low bias current (1 picoampere typically). Also, the temperature coefficient of the offset voltage becomes zero at some offset adjustment of the preamplifier. This offset can be countered by another offset produced by the resistor network between the preamplifier and the operational amplifier. Therefore, by making two adjustments, the offset voltage temperature coefficient and the sample to hold offset error can almost be eliminated.

A JFET serves as an analog switch and is connected to a corresponding flag in the control by a buffer and switch driver. The design of the switch and switch driver is derived from several sources.[5,7,8]

2-6 Peak Detector

One of the main reasons for developing the sampling controller was to be able to reduce a train of action potentials to peak values and time intervals before conversion. This section describes the device which signals the controller when a peak occurs on a particular channel.

In myoelectric recordings there is often a substantial amount of so-called base-line noise. The peak detector should therefore contain a threshold facility so that this type of interference can be rejected. In addition, a feature is required where either positive or negative peaks can be selected. Figure 2-15 shows in block diagram form how these minimum requirements can be met. The inverter enables negative peaks to be treated in the same way as positive peaks. The rectifier, with an adjustable level, slices off the bottom part of the waveform thus reducing noise problems. Finally, a comparator squares the

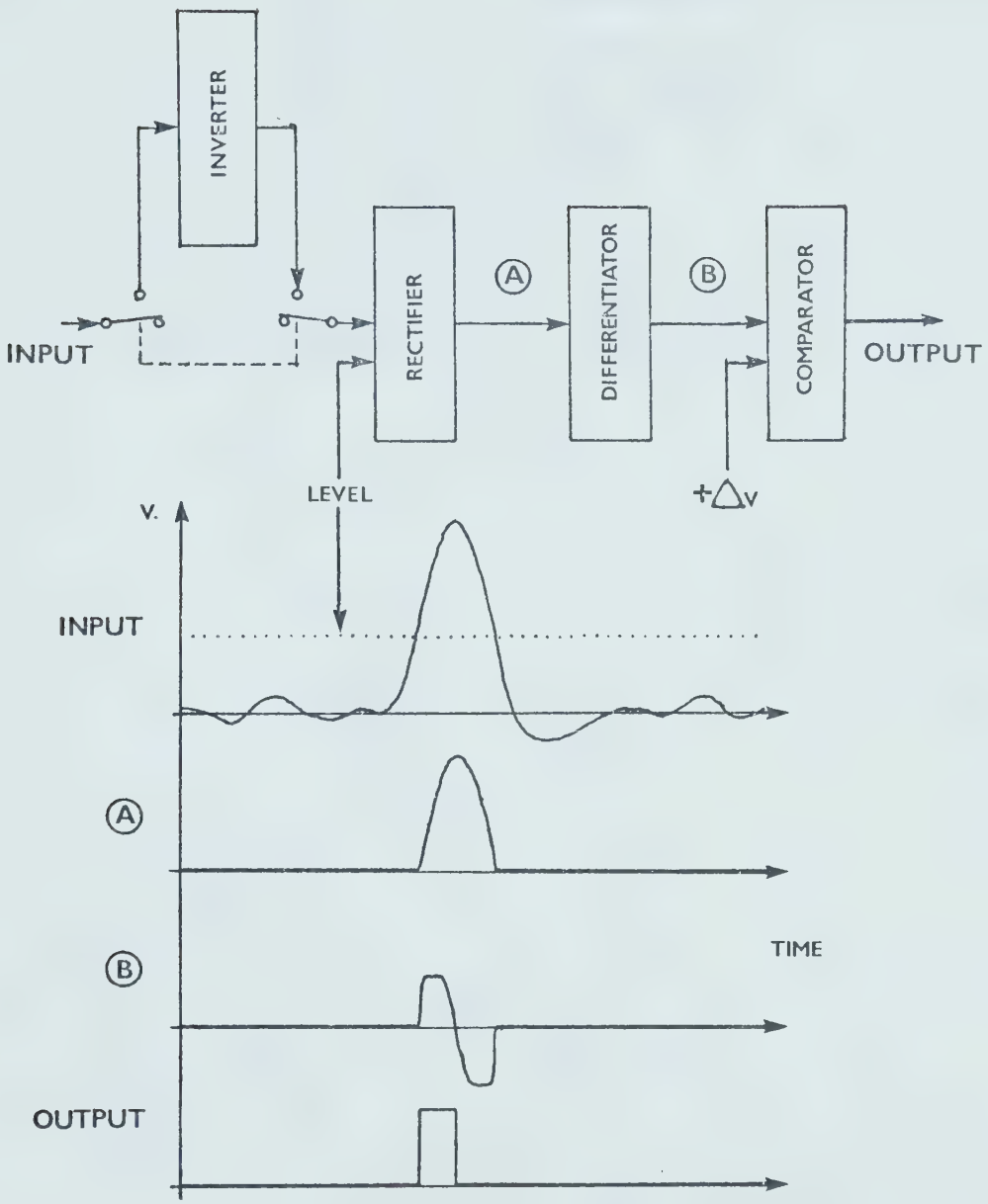


Figure 2-15 Operations of the peak detector.

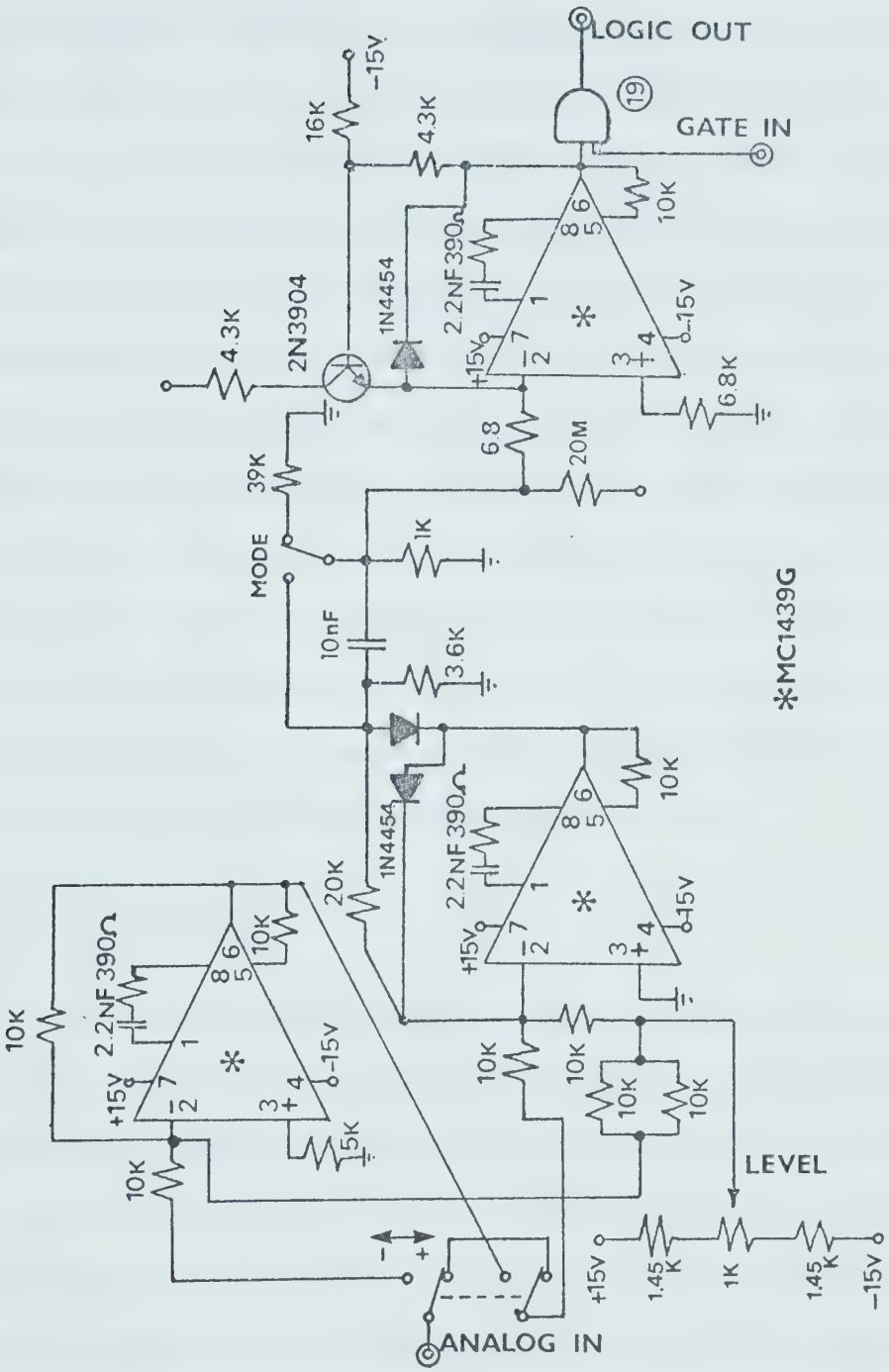


Figure 2-16 The peak detector.

derivative of the rectified signal. Recall that the flags in the control are set by a negative going transition at the appropriate sample command inputs. Therefore, the peak detector can be used to set a flag when a peak occurs on a corresponding analog channel.

The peak detector is shown in Figure 2-16. Operational amplifiers are connected in different configurations to act as the inverter, rectifier, and comparator. Signal differentiation is accomplished by a simple RC circuit. A three position switch allows for two different ranges of pulse widths in the peak mode as well as a capability for level gating. In the latter case, the capacitor is shorted out, thus eliminating the derivative function. Therefore the whole circuit acts as a level detector. Another feature of the peak detector is the AND gate at the output. It is especially useful in the level mode where it can gate a train of pulses whenever the waveform is above (or below) some artibrarily selected level.

2-7 The Oscillator

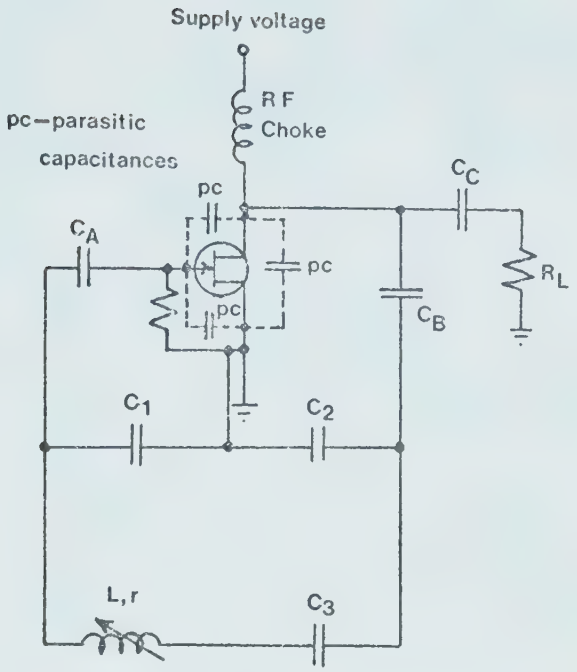
The oscillator supplies timing pulses to the control section as well as clock pulses to the timer. While the frequency of the oscillator is limited by the propagation delays of the logic in the control, the exact frequency that it must produce is determined only by the timer. That frequency is 1.024 MHz. The reason for such a peculiar figure is that the timer has a ten digit binary counter which divides by 1024. The first range of the timer is then a convenient number because the clock frequency of 1.024 MHz. is divided by 10 and 1024 to yield exactly 100 Hz. Therefore the ten digit counter fills up in 10 milliseconds.

The stability requirement is also determined mainly by the

timer. For accurate timing, the frequency must not vary more than ± 500 Hz. which corresponds to a .1% change. Even if the variation, for a conservative design, is limited to 0.05% it is clear that a crystal controlled oscillator could easily meet this specification. However, a less expensive oscillator without a crystal, such as the Clapp-Gouriet oscillator, can also meet this stability requirement.[9,10,11]

The Clapp-Gouriet oscillator was chosen because it is simple, quite stable, and frequency adjustable. In order to achieve frequency stability, each component in the oscillator that affects frequency must be stable. In addition, it is advantageous to make the frequency dependent on as few components as possible. Figure 2-17 shows a diagram of the Clapp-Gouriet oscillator as well as some important relationships. The parasitic capacitances of the JFET are dependent on temperature and power supply voltage. However, the frequency is only slightly affected by changes in the parasitic capacitances if C_1 and C_2 are made large with respect to them. A change in R_L also affects the frequency but this can be minimized by using a buffer amplifier to drive the load. Also, when $R>>r$ the temperature dependence of r_d is only weakly reflected in the frequency. If C_1 and C_2 are made large with respect to C_3, the frequency is mainly determined by L and C_3. Therefore it is important that these components be stable. For temperature stability, the capacitance C_3 is the worst offender. A combination of capacitances with opposite temperature coefficients reduces this problem.

Figure 2-18 shows the final design of the oscillator, buffer amplifier and clock pulse shapers.

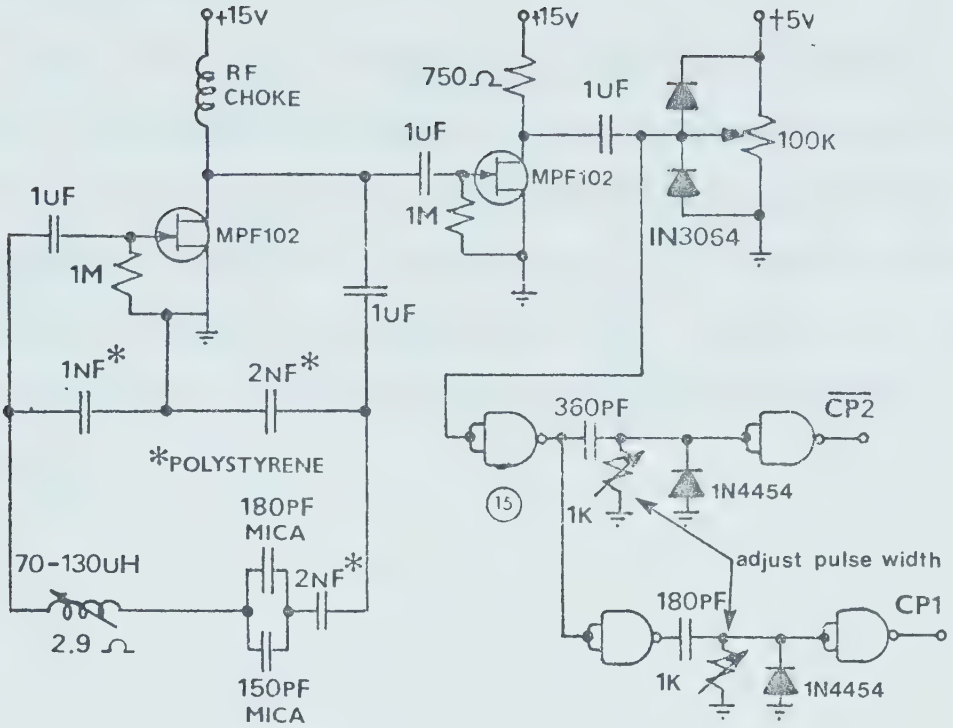


Oscillation frequency $$\omega^2 = \frac{1}{LC}\left[\frac{r\,C}{RC_2} + 1\right]$$

Self-starting condition $$g_m \geq \frac{r}{L}\left[C_1 + C_2 + \frac{C_1 C_2}{C_3}\right] + \frac{C_1}{R\,C_2}$$

where $R = r_d \| R_L$, $C = \dfrac{C_1 C_2 C_3}{C_1C_2 + C_1C_3 + C_2C_3}$, r_d = JFET drain resistance

Figure 2-17 The Clapp-Gouriet oscillator - the equations are derived using the Barkhausen criterion.[12]



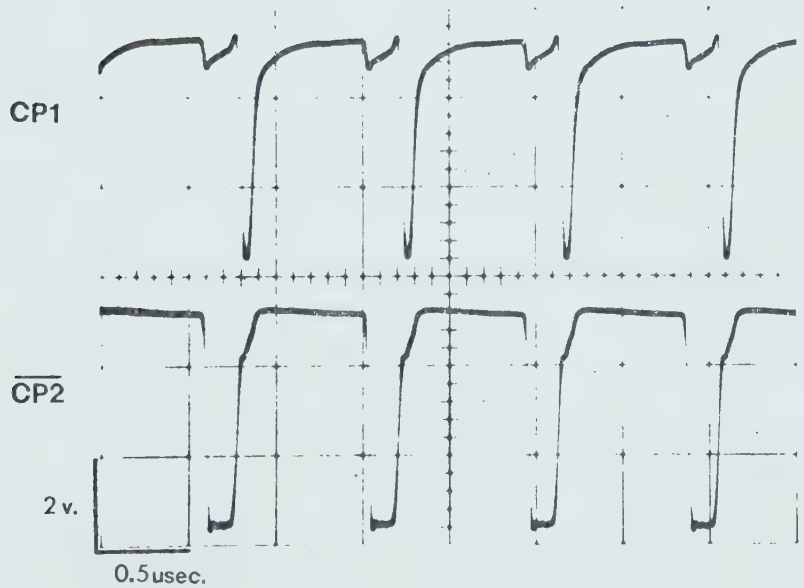


Figure 2-18 Oscillator and clock pulse shaper.

2-8 The Power Supplies

Three power supply voltages are needed by the Sampling Controller. The positive and negative 15 volt supplies are required by the analog circuits, while the positive 5 volt supply powers the digital circuits. Two transformers in parallel are needed for the 15 volt supplies, and two 5 volt regulators are used because of the large current requirements. A diagram of the power supplies is shown in Figure 2-19.

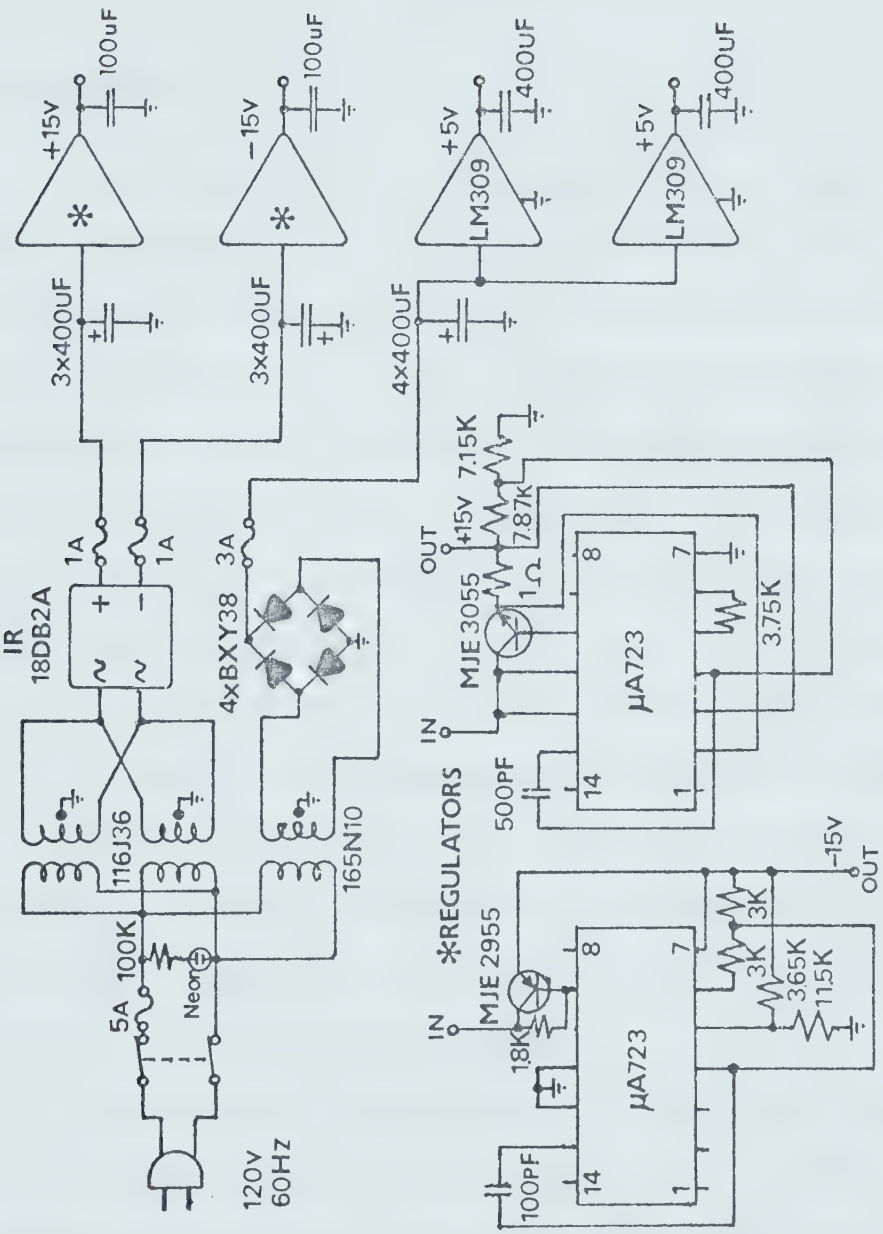


Figure 2-19 Power supplies.

Chapter 3

RESULTS

3-1 Construction

A considerable amount of attention has been given to the placement of the circuits in the Sampling Controller. Most of the digital circuits are in one rack while the analog circuits are separated from them, in another rack. This separation is very important because analog circuits are quite sensitive to transients generated by the logic devices. For the same reason, the regulators of the ± 15 volt supplies, for the analog circuits, are shielded and placed in the analog rack. The logic rack is placed above the analog rack, rather than the other way around, to avoid heating the analog circuits by convection currents.

The digital integrated circuits are mounted on cards that can be easily removed from the upper rack. The upper rack also houses the oscillator as well as the transformers, rectifiers, and filters for the power supplies. Enough space remains in the rack for the future expansion of the memory and time buffers.

For convenience and expandability, the analog circuits in the lower rack are constructed in modular form. There are five modules in all. Two are identical and contain four sample-hold circuits each. Another module has two peak detectors. The fourth contains the 15 volt regulators, and the switch drivers for the sample-hold circuits. The last module is empty to allow for the addition of more sample-hold circuits, peak detectors, or other related circuits. All of the modules

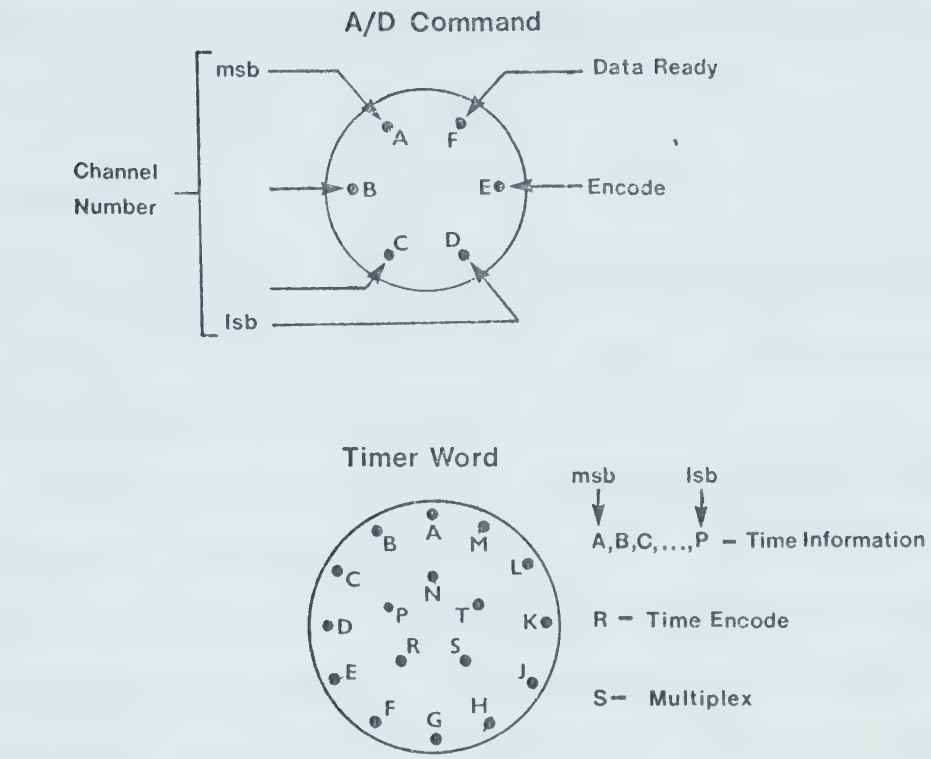


Figure 3-1 Connectors

are separated from each other by grounded shields.

In total, the Sampling Controller contains 171 digital integrated circuits, 30 integrated operational amplifiers, and 22 transistors.

3-2 Performance

The specifications for various parts of the controller are listed in tables 3-1, 3-2, and 3-3. In all cases the specifications apply over the temperature range from 0°C. to 50°C.

The maximum sampling rate, for a particular channel, under various conditions, may be found using Table 3-3. To illustrate, consider the case where the first 6 channels are used and where channels 1 and 3 are under memory control. The box containing the numbers 13.9 and 8.0 is located using the two facts that M = 2, and N = 6. The maximum sampling rate for a channel not under memory control is 13.9 KHz., while 8.0 KHz. is the maximum sampling rate for the two channels that are under memory control. Notice that the use of the memory does not affect the sampling rate of those channels not controlled by it. An explanation of how these sampling rates are calculated is given in Appendix 1.

3-3 Operation

An effort has been made to keep the operating procedures of the Sampling Controller simple. Convenience of operation was, in many instances, considered sufficient justification for added circuit complexity. For example, a special circuit was included to automatically clear the memory during power turn-on. Without this circuit the memory

Table 3-1 Specifications for Oscillator and Sample-Hold Circuits

Oscillator

Frequency	1.024 MHz. ± 250 Hz.
Stability-temperature	+ 1.0 Hz./°C
-time	± 5 Hz./day
-power supply	+ 15 v.-- + 2.5 Hz./volt (from 13v. to 17v.)
	+ 5 v.-- + 4.0 Hz./volt (from 4.75v. to 5.25v.)
Adjustable	from 0.91 MHz. to 1.36 MHz.

Sample-Hold

Acquisition Time	5.5 μsec. maximum (to within 2.5mv. of final value).
Aperture Time	300 nsec. maximum
Drift in Hold	2 mv./sec. maximum
Gain	1.0
Gain Accuracy	0.1%
Offset Voltage	Adjustable to zero; 10 μv./°C maximum
Input-impedence	1 Megohms minimum
-operating voltage	± 2.5 volts within specifications
-maximum voltage	± 15 volts
Output-impedence	0.3 ohms. maximum
-load current	15 ma. maximum
-short circuit duration	continuous
Logic input	DTL/TTL compatible
	low-sample, high-hold

Table 3-2 Specifications for Peak Detector and Power Supplies

Peak Detector

Pulse height - SLOW.....	.5v min, 2.5v max.
- FAST.....	.5v min, 2.5v max.
Pulse width - SLOW.....	2 msec. min., 20 msec. max.
- FAST.....	.3 msec. min., 2 msec. max.
Input Impedence.....	10 K.
Peak Detector Delay.....	12 μsec. max. - FAST; 40 μsec. max. - SLOW
GATE IN.....	DTL/TTL compatible low-inhibit; high; admit
LOGIC OUT.....	DTL/TTL compatible 1 to 0 transition indicates peak.
LEVEL Mode.....	Recommended analog operation to 2 KHz; resolution 2 mv.

Power Supplies

± 15 Volt

Voltage.....	within 1% of nominal voltage
Current.....	1 amp. maximum
Temp. Coefficient.....	.015%/°C
Regulation - Line.....	1 mv. for 105 to 125 v. rms input
- Load.....	15 mv./amp. of load current

+ 5 Volt

Voltage.....	within 2% of nominal voltage
Current.....	1.5 amp. (each regulator) maximum
Temp. Coefficient.....	.02%/°C
Regulation - Line.....	3 mv. for 105 to 125 v. rms input
- Load.....	50 mv./amp. of load current

Table 3-3 Maximum Sampling Rate

Total Number of Channels Scanned (N)	Number of Channels Under Memory Control (M)				
	0	1	2	3	4
1	83.0 / –	– / 62.5	– / –	– / –	non-memory / memory
2	41.5 / –	41.5 / 35.7	– / 34.4	– / –	– / –
3	27.6 / –	27.6 / 25.0	27.6 / 18.8	– / 22.7	– / –
4	20.7 / –	20.7 / 19.2	20.7 / 13.0	20.7 / 12.5	– / 16.4
5	16.6 / –	16.6 / 15.6	16.6 / 9.9	16.6 / 8.6	16.6 / 9.1
6	13.8 / –	13.8 / 13.1	13.8 / 8.0	13.8 / 6.5	13.8 / 6.3
7	11.8 / –	11.8 / 11.2	11.8 / 6.7	11.8 / 5.3	11.8 / 4.8
8	10.4 / –	10.4 / 10.0	10.4 / 5.7	10.4 / 4.4	10.4 / 3.9

All rates in kilohertz.

See Appendix 1 for derivation.

would have to be cleared manually by momentarily turning all the front panel switches off.

Operation without memory. The only restriction in this situation is a maximum sampling rate. The worst case occurs when 8 channels are in use yielding a maximum sampling rate, per channel, of 10.4 KHz. Without the Sampling Controller, the analog-to-digital converter can sample 8 channels at a maximum rate of 12.5 KHz. Even with this 17% reduction, however, the Sampling Controller allows sampling rates that are more than adequate for most physiological experiments.

It should always be remembered that it is not wise to scan channels that are not in use. For instance, if the first three channels are being scanned, and only channels 1 and 2 are used, it would be better to turn the END CHANNEL selector to 2 instead of 3. By doing this a slight increase in the maximum sampling rate, for channels 1 and 2, can be attained.

Operation with memory. Any of the first four channels may be controlled by the memory simply by putting the appropriate switch on. When one or more of the switches are on, an orange light above the switches glows, indicating that the memory is in use. The sampling rate limitation for the channels which are under memory control is more severe than for those which are not (Table 3-3).

Only channels that are being scanned should be under memory control. For example, switches 3 and 4 should not be on if the END CHANNEL selector points to 2. If the END CHANNEL selector is on N and switch N+1 is on, all 16 channels will be scanned instead of the first N.

Whenever the memory switches are on, the timer is also in operation. Since the oscillator frequency is crucial to the accuracy of the timer, the frequency should be checked at least every 180 days. If the frequency is not 1,024,000 ± 250 Hz., the adjustment screw on the oscillator card should be turned until the frequency is within this range.

Sample-hold circuits. Periodically the offset of the sample-hold circuits should be checked. To do this, the input of the sample-hold circuit should be grounded, and the offset adjusted until the analog-to-digital converter indicates zero volts. When the FET input preamplifiers were installed, the sample-hold circuits were adjusted for near zero temperature coefficient of the offset voltage. This was done by heating the modules in an oven and turning the temperature coefficient potentiomenters until a minimum change was noted in the offset voltage for each circuit. (Changes of less than 5 microvolts per centigrade degree can typically be achieved.) The same procedure should be followed if, for any reason, the preamplifiers are replaced.

Peak detector. The front panel controls of the peak detector module are shown in Plate 1. In the peak mode, a 1 to 0 transition appears at LOGIC OUT when a peak occurs at ANALOG IN.

Several options are available in the peak mode. First, the polarity switch (indicated by ±) allows either a positive or negative peak to be detected. A positive peak is one with a negative second derivative. Second, the LEVEL knob allows some discrimination of signal peaks on the basis of amplitude. When the polarity switch is up (+) any peaks below the LEVEL voltage are ignored. The reverse is true if the

polarity switch is down. Third, the response of the peak detector may be changed according to the anticipated width of the pulses. If pulses between .3 milliseconds and 2 milliseconds in duration are expected, the mode switch should be in the up position (FAST). The mode switch should be in the intermediate position (SLOW) if the pulses are between 2 milliseconds and 20 milliseconds long. The FAST mode is especially suitable for neuro-electric action potentials.

The peak detector is in the level mode when the mode switch is down. In this mode, if the polarity switch is up, LOGIC OUT is high when ANALOG IN is above the LEVEL voltage. On the other hand, if the polarity switch is down, LOGIC OUT is high when ANALOG IN is below the LEVEL voltage. This facility is useful if, for example, the period of a waveform is to be measured. In other cases, it may be necessary to sample a waveform at a high rate when the waveform is above or below a certain value. For example, it may be desirable to sample an amplified action potential at 25 KHz. but only when its amplitude is above 0.5 volts. In this situation, the polarity switch should be up, the LEVEL knob should indicate + 0.5 volts, the mode switch should be on LEVEL, and a 25 KHz. square wave should be applied to GATE.

Typical results. Figure 3-2, 3-3, and 3-4 show examples of computer data acquired using the analog-to-digital converter and Sampling Controller.

The channel numbering on the Sampling Controller starts at 1 instead of 0 so that the binary channel number 0000 indicates channel 1; 1111 indicates channel 16, and so on.

The most significant bit of the converter output word is the sign bit; 1 indicates minus, and 0 indicates plus. Negative numbers

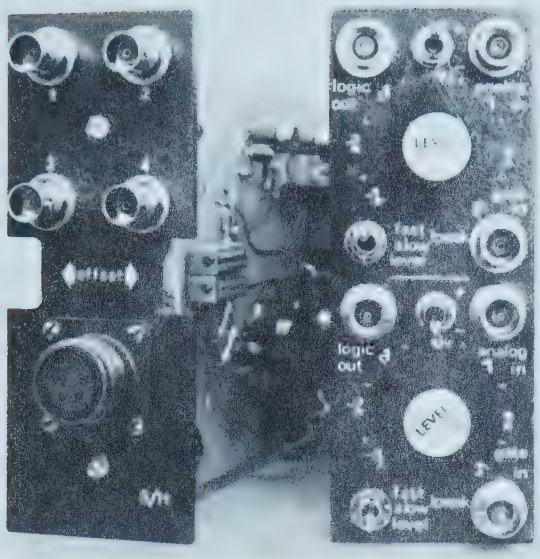


Plate 1 Modules: A sample-hold module (left), and peak detector module.

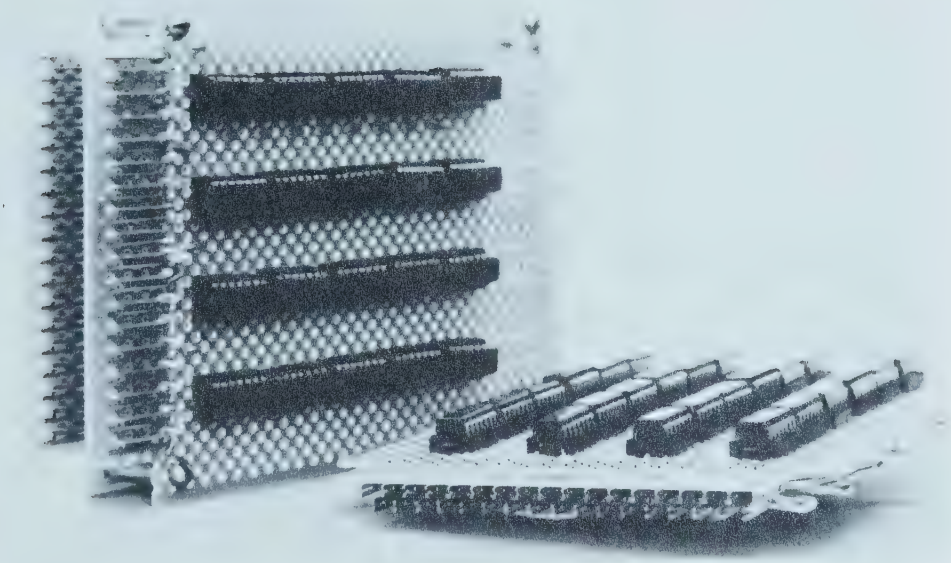


Plate 2 Logic Cards, The double card assembly is the control and the single card is the sub-memory.

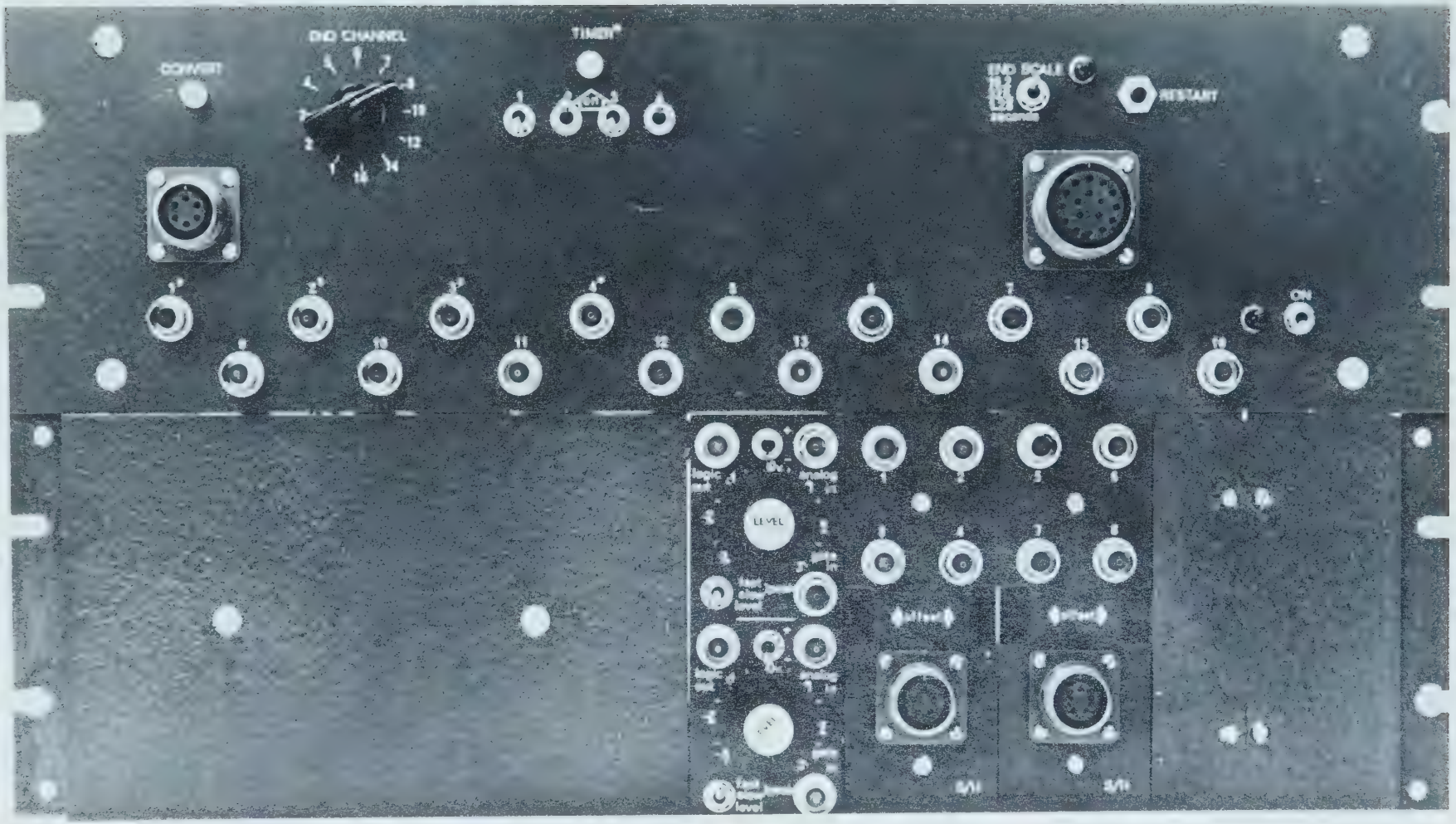


Plate 3 The Sampling Controller

```
0000000000 0000
0000000000 0000
0000000000 0000
0000000000 0000
0000000000 0000
0000000000 0000
0000000000 0000
0000000000 0000
0000000000 0000
0000000000 0000
0000000000 0000
0000000000 0000
0000000000 0000
0000000000 0000
0000000000 0000
0000000000 0000   (a)

0000000010 0000
0000000011 0001
0000000100 0010
0000000011 0011
1110111000 0011
1110111000 0000
1110111000 0001
1110111000 0010
1101110000 0000
1101101110 0001
1101101110 0010
1101101101 0011
1101110000 0000
1101101111 0001
1101110000 0010
1101101111 0011   (b)
```

```
0000000000 0000
1110010100 0100
1110110100 0101
1110110100 0101
1110010100 0100
1110010100 0100
1110110100 0101
1110010100 0100
1110110100 0101
1110010100 0100
1110110100 0101
0000000000 0000
1110110100 0101
1110010100 0100
1110010100 0100
1110110100 0101
1110010100 0100
1110110100 0101
1110010100 0100
1110110100 0101
0000000000 0000    (c)
     ↑         ↑
Converted   Channel
Voltage     Number
```

Figure 3-2 Sections of typical computer print-outs of data generated by the data acquisition system--analog-to-digital converter information: (a) channel 1 grounded and sampled at 1 KHz.; (b) channels 1, 2, 3, and 4 simultaneously sampling a 1 volt triangle wave at 10 KHz.; (c) channel 1 grounded and sampled at 100 Hz., channels 5 and 6 floating and sampled (simultaneously) at 500 Hz.

0000000000 0001	0000000000 0001
1110111000 0010	1110111000 0010
0000000000 0001	0000000000 0001
1110111000 0010	0000000000 0001
0000000000 0001	1110111000 0010
1110111000 0010	0000000000 0001
0000000000 0001	1110111000 0010
1110111000 0010	0000000000 0001
0000000000 0001	1110111000 0010
1110111000 0010	0000000000 0001
0000000000 0001	1110111000 0010
1110111000 0010	0000000000 0001
0000000000 0001	1110111000 0010
1110111000 0010	0000000000 0001
0000000000 0001	1110111000 0010
1110111000 0010	1110111000 0010
0000000000 0001	0000000000 0001
1110111000 0010	1110111000 0010
0000000000 0001	0000000000 0001
1110111000 0010	1110111000 0010
0000000000 0001	0000000000 0001
1110111000 0010	1110111000 0010
0000000000 0001	0000000000 0001
1110111000 0010	1110111000 0010
0000000000 0001	0000000000 0001
1110111000 0010	1110111000 0010
0000000000 0001 (a)	0000000000 0001 (b)

Figure 3-3 Sections of typical computer print-outs of data generated by the data acquisition system illustrating the use of the memory: (a) memory on-channel 2 sampled 6 microseconds after channel 3 at 1 KHz. (channel 2 is grounded and channel 1 is floating); (b) memory off-same conditions as (a). Note how the order is mixed up in (b).

```
1010000000 0100
1010000000 0100
1010000000 0100
1010000000 0100
1010000000 0100
1010000000 0100
1010000000 0100
1010000000 0100
1010000000 0100
1010000000 0100   (a)
```

Decimal Equivalent = $5/8 \times (2^4 \times 10)$ msec.

= 100 msec.

```
1001111001 0100
0001111010 0000
1001111001 0100
0001111010 0000
1001111001 0100
0001111010 0000
1001111001 0100
0001111010 0000
1001111001 0100
0001111010 0000   (b)
    ↑         ↑
Fraction   Exponent
```

1001111001 0100 = 1001111001 0100

+

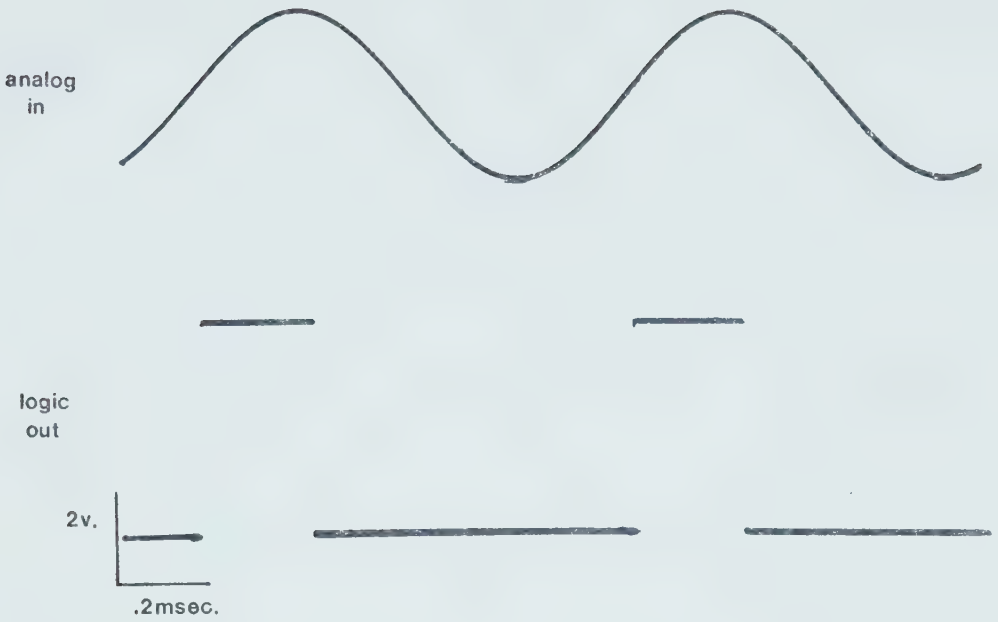
0001111010 0000 = 0000000111 0100

1010000000 0100

Figure 3-4 Sections of typical computer print-outs of data generated by the data acquisition system--timer information: (a) times between pulses at a steady frequency of 10 Hz.: (b) channels 1 and 2 are sampled at 10 Hz but channel 1 is sampled about 1.2 milliseconds after channel 2. Note that the total of the time intervals equals 100 milliseconds which corresponds to 10 Hz.

are simply a binary two's complement of positive numbers. (The binary two's complement of a number is just the one's complement plus one.) For example, the voltage -2.5 volts corresponds to 1,000,000,000. The resolution of the converter is 4.88 millivolts.

Figures 3-5 and 3-6 are photographs of oscilloscope displays showing the operation of a peak detector and sample-hold circuit.



(a) Peak mode (+, FAST, LEVEL = 0v.)

(b) Level mode (+, GATE = 2KHz., LEVEL = 1.8v.)

Figure 3-5 A peak detector in operation.

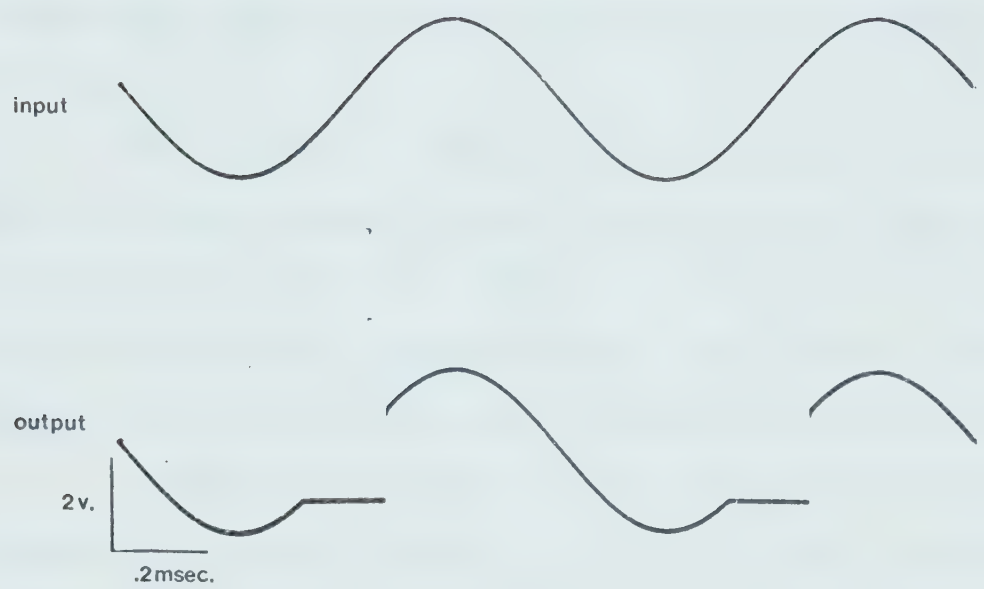


Figure 3-6 A sample-hold circuit (hold period = 0.2 msec.).

Chapter 4

SUMMARY

The Sampling Controller is presented, in this thesis, as an aid to real-time analysis. In many situations, it can reduce the quantity of superfluous data sent to the computer by an analog-to-digital converter.

The Sampling Controller makes a 16 channel multiplexed analog-to-digital converter appear like 16 independent single channel analog-to-digital converters. Therefore, the channels may be sampled at different rates, or even simultaneously. The regular or irregular sampling rate for a channel is determined by an external pulse source.

A timer has been built into the controller so that the times between the occurances of samples, on any of the first four channels, can be measured. This timer, in conjunction with one of the included peak detectors, provides a means whereby a series of action potentials can be reduced to peak values and interpeak time intervals.

For test purposes the Sampling Controller was connected to a Hewlett-Packard 5610A analog-to-digital converter and 2100A computer. Various channels were sampled at different rates and a number of channels were sampled simultaneously. The correct operation of the timer was verified by sampling several channels at known intervals. In each of these respects, the Sampling Controller performed satisfactorily.

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Appendix 1

MAXIMUM SAMPLING RATE

Following is an explanation of how the values of Table 3-3 are determined. It is always assumed that the END-CHANNEL selector of the controller points to the last channel in use. (For example, the selector should indicate 5, if the first 5 channels are in use.)

Let N = total number of channels scanned,

M = total number of channels under memory control,

t = interrogation time = 1 microsecond,

T = conversion time allowed by controller = 11 microseconds,

4t = cycle time of strobe counter in the memory.

Case #1 M = 0; N = 1,2,3,...,8

An examination of the timing of the control unit reveals that the time required to interrogate a flag, digitize a value, and advance to the next channel is (t+T). The longest period of time that can elapse between interrogations of a particular flag is N(t+T). This occurs when all flags are set simultaneously. Therefore,

$$\text{Maximum Rate} = R = \frac{1}{N(t+T)} \text{ Hz } (M=0)$$

$$= \frac{83}{N} \text{ KHz.}$$

Case #2 M = 1,2,3,4; $N \geq M$

The maximum sampling rate for a channel that is not under

memory control is $\frac{1}{N(T+t)}$ whether other channels are controlled by the memory or not. Therefore, this case is only concerned with those channels influenced by the memory.

To find the maximum sampling rate, the longest possible delay is determined which can exist between the arrival of a sampling pulse and the conversion of the corresponding channel. If the memory is used, the delay can arise from a number of sources which are described below.

(1) The strobe counter in the memory may delay the entering of information into the memory by as much as 4t.

(2) If the channel of interest is given the lowest priority in the memory, the delay for this channel is equal to or longer than any other channel under memory control.

(3) The position of the scan counter, when the memory associated flags are set, is also important. The worst situation occurs when the scan counter is interrogating the channel after the channel of highest priority in the memory. In this case the scan counter must make one complete cycle before converting even the channel of highest priority.

(4) The channels that are not controlled by the memory cause the maximum delay if they are sampled at the maximum rate possible. In other words the corresponding flags are set every time the control interrogates them.

(5) If the memory-associated channels are ranked in "reverse order", this necessitates one complete cycle of the scan counter between a conversion of each of them, and therefore more delay. Reverse order means an order opposite to the numerical order of the channels. For example, if channels 1, 2, and 3 are

ranked in reverse order the channel of highest priority is 3 and the one of lowest priority is 1.

(6) When the situation in (4) and (5) exists, the longest delay between the conversion of the memory-controlled channels occurs when they are grouped together.

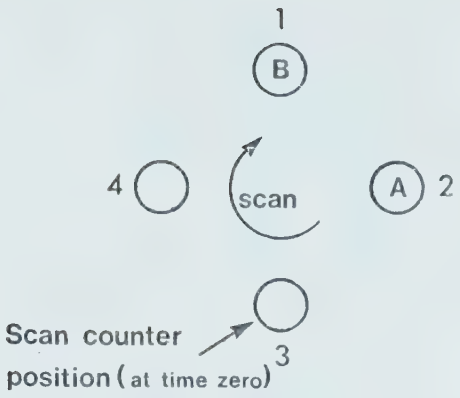
To illustrate the previous points the following example is provided (Figure A1-1). Four channels are in use but only two of these are under memory control. According to point (6), the worst cases for the arrangement of the memory-associated channels are 1, and 2; 2, and 3; 3, and 4; or 4, and 1. Since the operation of the scan counter is cyclic, there is no difference between these cases, so the arrangement of channels 1, and 2 may be chosen arbitrarily.

From (5) it is seen that channel one should be given the lower priority (B), and point (2) indicates that channel 1 is the worst case of the two.

The position of the scan counter is given by point (3) to be channel 3. Flags 3 and 4 should always be set to provide the maximum delay possible, according to (4).

At time zero flags 2, and 1 are set simultaneously but channel 2 is given the highest priority by the strobe counter in the memory. The total time until the end of the conversion of channel 1 is given in Figure A1-1.

The general case is given in Figure A1-2.

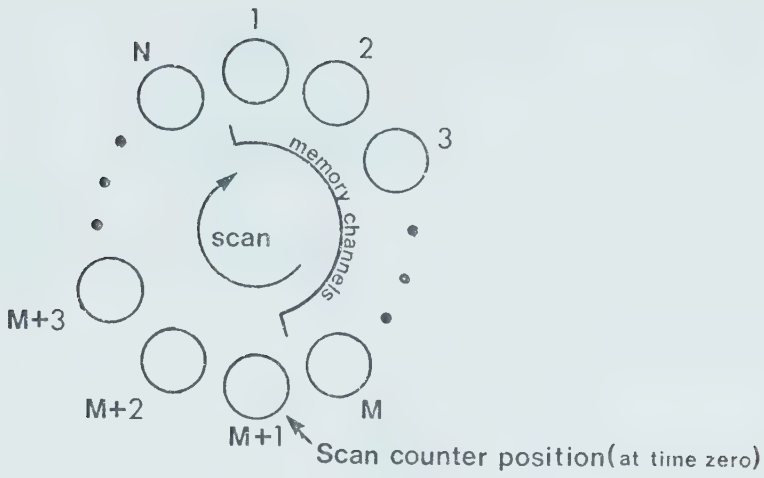


4t	...	strobe counter delay [point (1)]
(t+T)	...	conversion of channel 3
(t+T)	...	conversion of channel 4
t	...	interrogation of channel 1 which is blanked by the memory
(t+T)	...	conversion of channel 2
(t+T)	...	conversion of channel 3
(t+T)	...	conversion of channel 4
(t+T)	...	conversion of channel 1

$5t + 6(t+T)$

$$R = \frac{10^3}{5 + 6(12)} = 13 \text{ KHz.}$$

Figure A1-1 Example when $M \neq 0$.



4t	...	strobe counter delay
(N-M)(t+T)	...	conversion of non-memory channels
M-1 times: (M-1)t	...	interrogation of blanked channels
(t+T)	...	conversion of highest priority channel
(N-M)(t+T)	...	conversion of non-memory channels
(M-1)t	...	interrogation of blanked channels
(t+T)	...	interrogation of next highest priority channel
(N-M)(t+T)	...	conversion of non-memory channels
.		
.		
.		
(M-1)t	...	interrogation of blanked channels
(t+T)	...	conversion of next to lowest priority channel
(N-M)(t+T)	...	conversion of non-memory channels
(t+T)	...	conversion of lowest priority channel

$$(M^2-2M+5)t + (M-M^2+MN)(t+T)$$

Therefore, $$R = \frac{10^3}{(M^2-2M+5) + 12(M+MN-M^2)} = \frac{10^3}{12MN - 11M^2 + 10M + 5} \text{ KHz.}$$

Figure A1-2 The general case for $M \neq 0$.

Appendix 2

INTEGRATED CIRCUITS

Modified Diode Transistor Logic (MDTL)

Maximum Ratings

Supply Voltage		8.0 V.
Output Current (into outputs)	buffers	150 ma
	others	30 ma
Input Forward Current		-10 ma
Input Reverse Current	buffers	5 ma
	others	1 ma
Operating Temperature Range		0 to 75°C. (MC 830 Series)

Logic Levels

Logic 0	0.0 to 0.4 volts
Logic 1	2.5 to 5.0 volts

Code Number	Type	Function
1	MC 830	Expandable Dual 4-input NAND Gate
2	MC 833	Dual 4-input Expander
3	MC 834	Hex Inverter
4	MC 836	Hex Inverter
5	MC 837	Hex Inverter
6	MC 838	Decade Counter
7	MC 839	Divide-by-Sixteen Counter
8	MC 846	Quad 2-input NAND Gate
9	MC 849	Quad 2-input NAND Gate (2 K pullup resistor)
10	MC 851	Monostable Multivibrator
11	MC 852	Dual J-K Flip-Flop (common clock and C_D, separate S_D)
12	MC 853	Dual J-K Flip-Flop (separate clock and S_D, no C_D)
13	MC 855	Dual J-K Flip-Flop (common clock and C_D, separate S_D, 2K pull-up)
14	MC 856	Dual J-K Flip-Flop (separate clock and S_D, no C_D, 2K pull-up resistor)
15	MC 857	Quad 2-input Buffer
16	MC 861	Expandable Dual 4-input NAND Gate (2K pull-up resistor)
17	MC 1801	Dual 5-input NAND Gate (2K pull-up resistor)
18	MC 1803	Expandable 8-input NAND Gate (2K pull-up resistor)
19	MC 1806	Quad 2-input AND Gate
20	MC 1809	Quad 2-input OR Gate (2K pull-up resistor)
21	MC 1813	Quad Latch
22	MC 1814	Quad Latch

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